Status of the TBM

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Functions

- Control readout through token pass
- Maintain event syncronization
- Pass coded trigger information to ROC's
- Stack triggers awaiting token pass
- Discard triggers if too many stacked up
- Write event header and trailer
- Act as hub for I^2C commands

Components

- L1 decoder
- outgoing trigger encoder
- 4-bit trigger counter
- 4-bit stack counter
- 4-bit stack overflow counter
- 16-deep token stack containing
  4-bit trigger number and
  4-bit header status
- token out bit
- header status register (4 bits)
- trailer stqatus register (4 bits)
- calibratin bit
- 2-bit DAC
- I^2C interface

$\boxed{\text{Stack Depth}}$

How deep should stack be?

- Guiding principle:

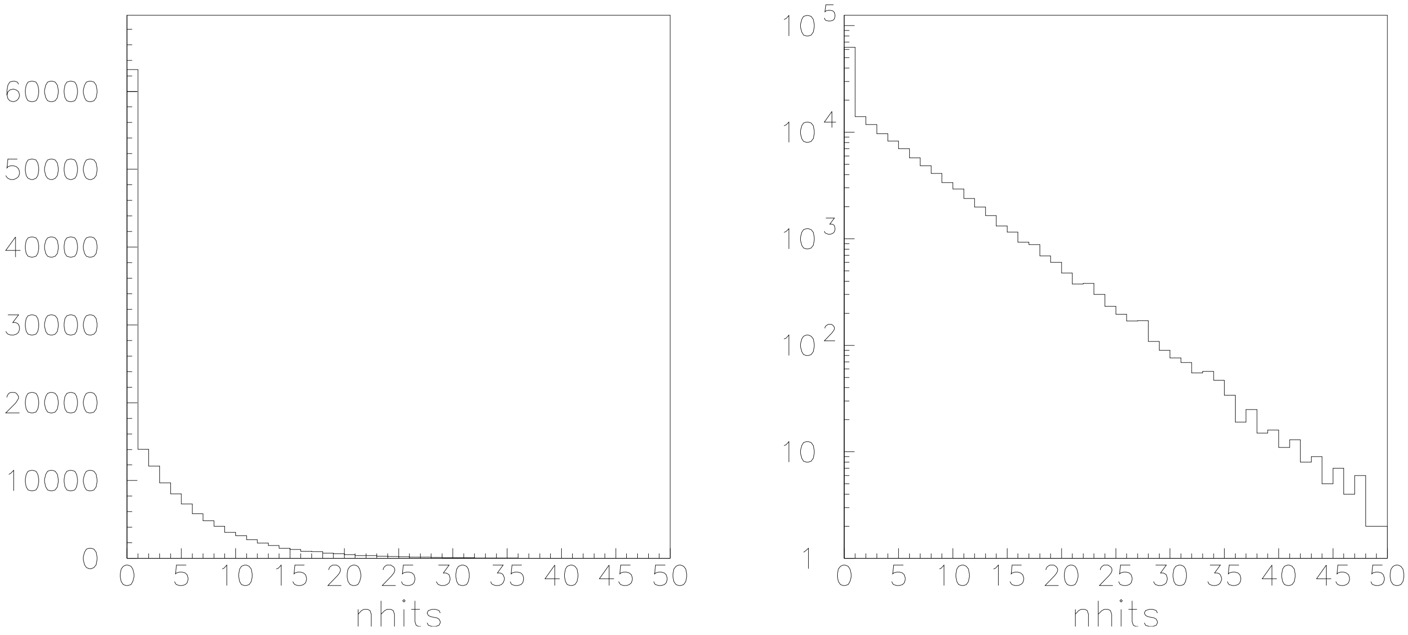
  $<$ 0.1% event loss at twice anticipated trigger rate

  $\Rightarrow$ $\boxed{< 0.1\% \text{ loss at 200 kHz}}$

- study 7 cm layer at full luminosity
- use parameterized hit distributions from Danek (1 year old)
- Assumptions

  $\rightarrow$ 20 MHz readout rate

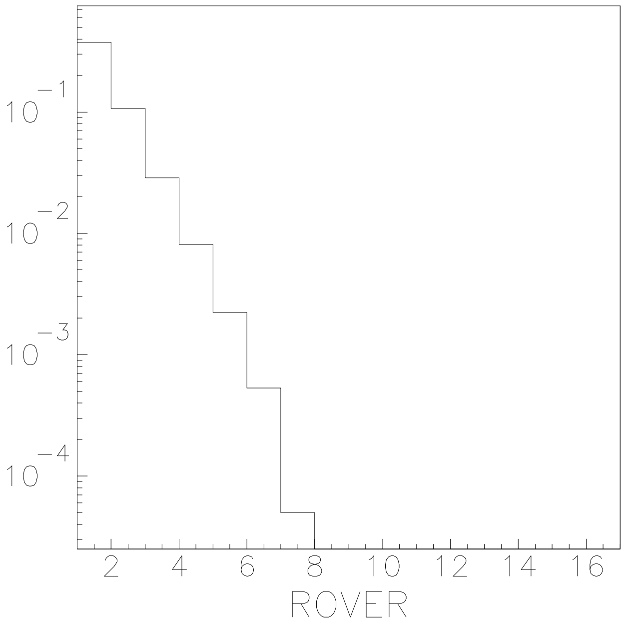
  $\rightarrow$ Number of clock cycles per event = header+trailer+8*nchips+8*nhits = 8 + 8 + 8*4 + 8*nhits

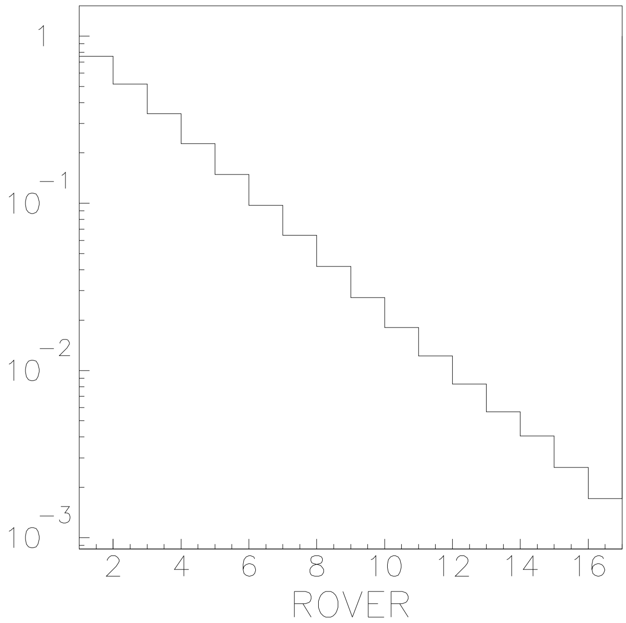


- 7 cm layer full luminosity
- 4 σ noise
- 42% no hits
- average number of hit = 3.6

100 kHz

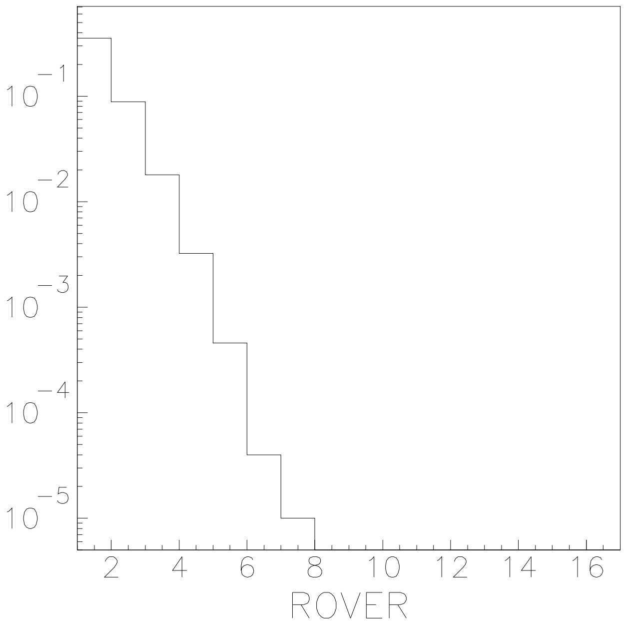
200kHz

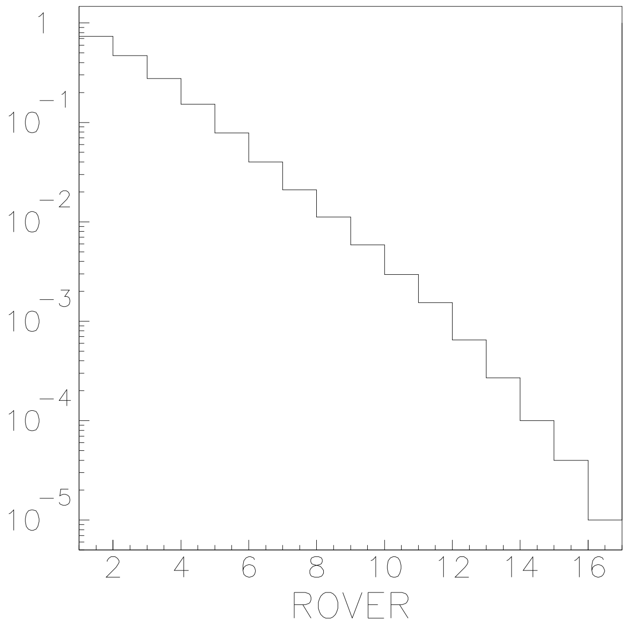




$\leq$8 triggers in 40 μs

$\leq$8 triggers in 20 μs





$\rightarrow$ Conclusions

- Stack depth for $\leq$ 0.1% data loss

L1 Rate	Extra Rule	Stack Depth
100 kHz	none	6
100 kHz	$\leq$ 8 in 40 μs	5
200 kHz	none	16 (0.2%)
200 kHz	$\leq$ 8 in 20 μs	12

- Stack depth of 8 more than sufficient for 100 kHz
- For 200 kHz need stack depth of 16
- Design for depth of 16
- If design constraints cut back

Trigger Codes

$\rightarrow$ incoming L1 trigger

- incoming L1 coded in 3 clock pulses

100	normal
101	synchronize (pre-pulse in ROC pulsing mode)
110	orbit gap clear
111	empty orbit clear and calibrate

$\rightarrow$ outgoing trigger to ROC's

- Trigger line 1

100	(not used)	
101	normal	increment trigger counter latch event for readout
110	no readout	increment trigger counter event not latched
111	pre-pulse	load ROC calibration

- Trigger line 2

100	(not used)	
101	synchronize	reset trigger counter
110	orbit-gap	clear column readout
111	empty orbit	clear readout buffers

Header/Trailer Structure

Header

- Black
- Black
- Trigger number at time L1 arrived (2 MSB's)
- Trigger number at time L1 arrived (2 LSB's)
- Header status word (2 MSB's)
- Header status word (2 LSB's)
- Stack overflow counter (2 MSB's)
- Stack overflow counter (2 LSB's)

Trailer

- White
- White
- Trigger number at time of token return (2 MSB's)
- Trigger number at time of token return (2 LSB's)
- Trailer status word (2 MSB's)
- Trailer status word (2 LSB's)
- Stack counter (2 MSB's)
- Stack counter (2 LSB's)

Event Synchronization

- TBM will contain a 4-bit trigger counter
- contents of this counter at time of arrival of L1 trigger will be reported in frame header of token pass associated with trigger
- ROC's will report contents of 4-bit trigger counters corresponding to event being readout
- upon receipt of "synchronize' L1 trigger, trigger counters in TBM and in ROC's will be reset
- event status code bit will be set in frame header indicating that this was a synchronize event
- in normal operation "synchronize' L1 trigger will arrive every 64th event
- if TBM trigger counter is not 1111 when "synchronize' L1 trigger is received an event status code bit will be set in frame header

Token Pass

- only one token is out at any time
- token is sent out either when L1 arrives (if no token passes are on stack) or when previous token returns (if there are token passes on stack)
- there is one token pass for each L1 trigger (except those for which readout is blocked)
- during token pass, events for L1 corresponding to that token pass as well as any subsequently triggered events will be readout
- as a result of the above, some token passes will not contain any data

I^2C Commands

- reset
- set token stack maximum
- report contents of counters
- report contents of stack
- program for calibration
- program for ROC pulsing
- enable/disable passing of triggers

Status Bits

- Header Status Bits

  Bit 1 – synchronization clear trigger

  Bit 2 – orbit gap clear trigger

  Bit 3 – empty orbit clear trigger

  Bit 4 – trigger counter synch. error

- Trailer Status Bits

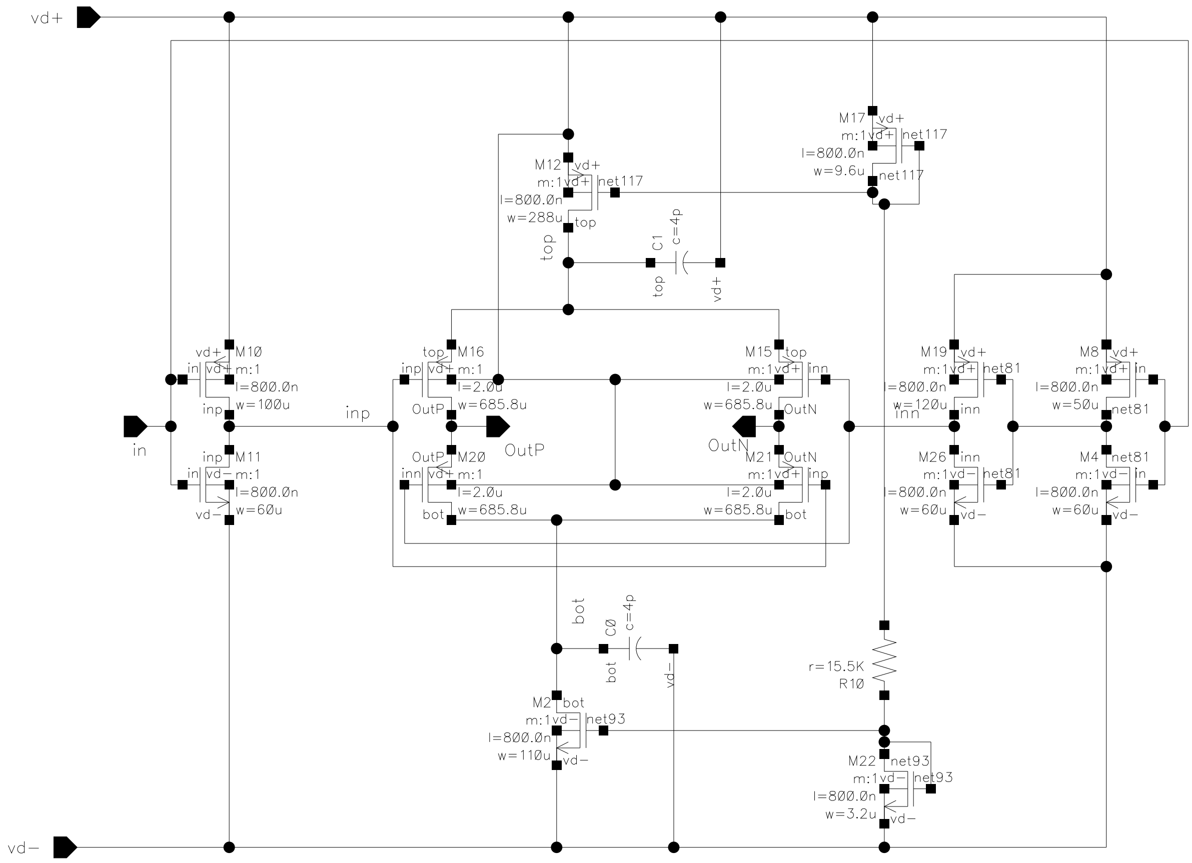
  Bit 1 – ”no readout“ trigger issued

  Bit 2 – synchronization trigger issued

  Bit 3 – empty-orbit trigger issued

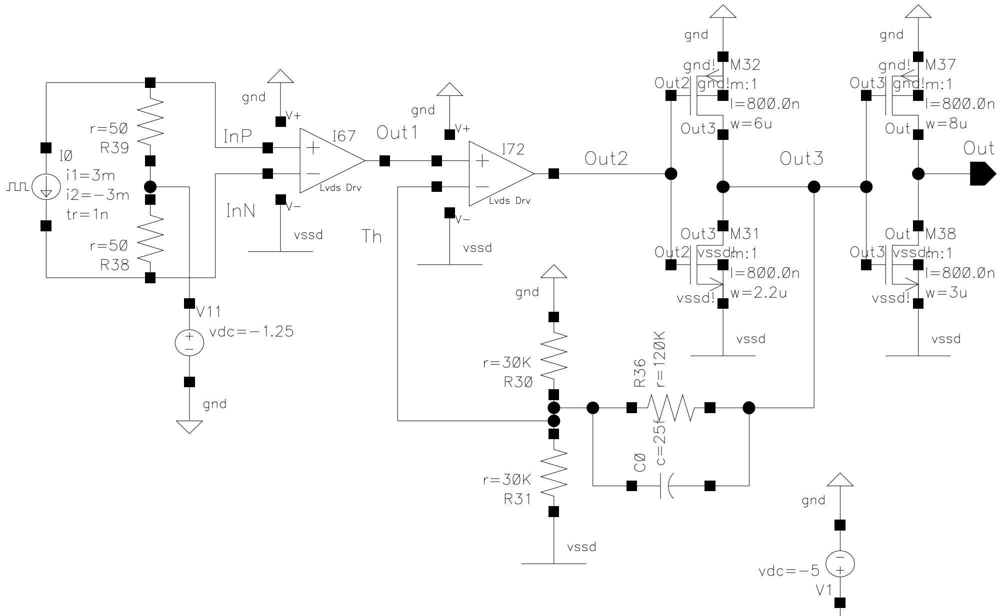
  Bit 4 – (not used)

LVDS Driver

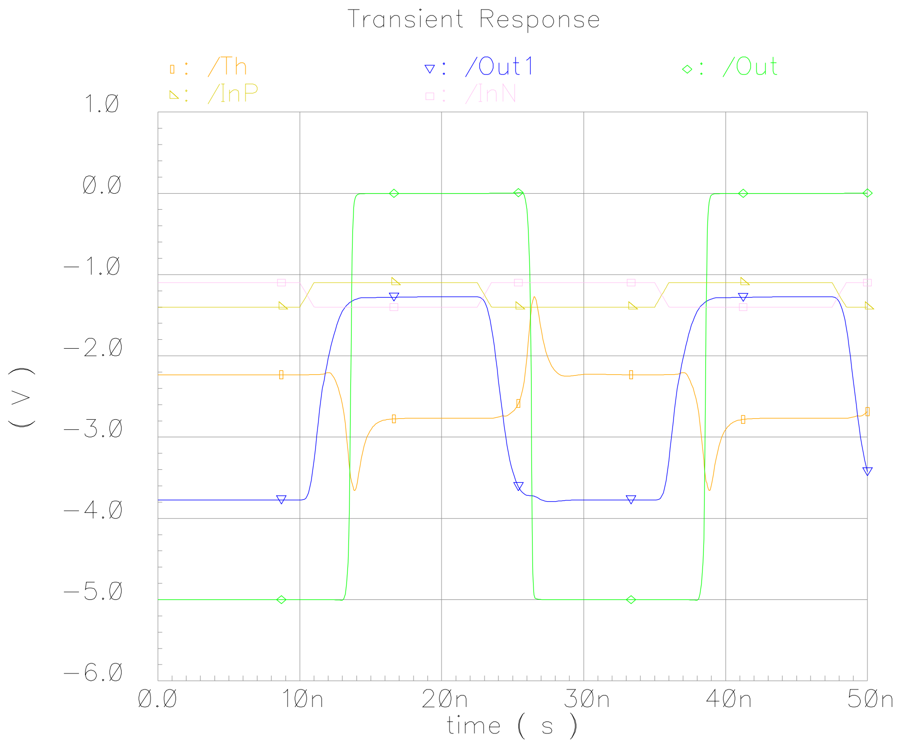


- $\pm$ 3.5 mA driver
- V_{out} centered on -1.25 V
- no back termination
- Power = 3.5 mA $\times$ 5 V = 175 mW

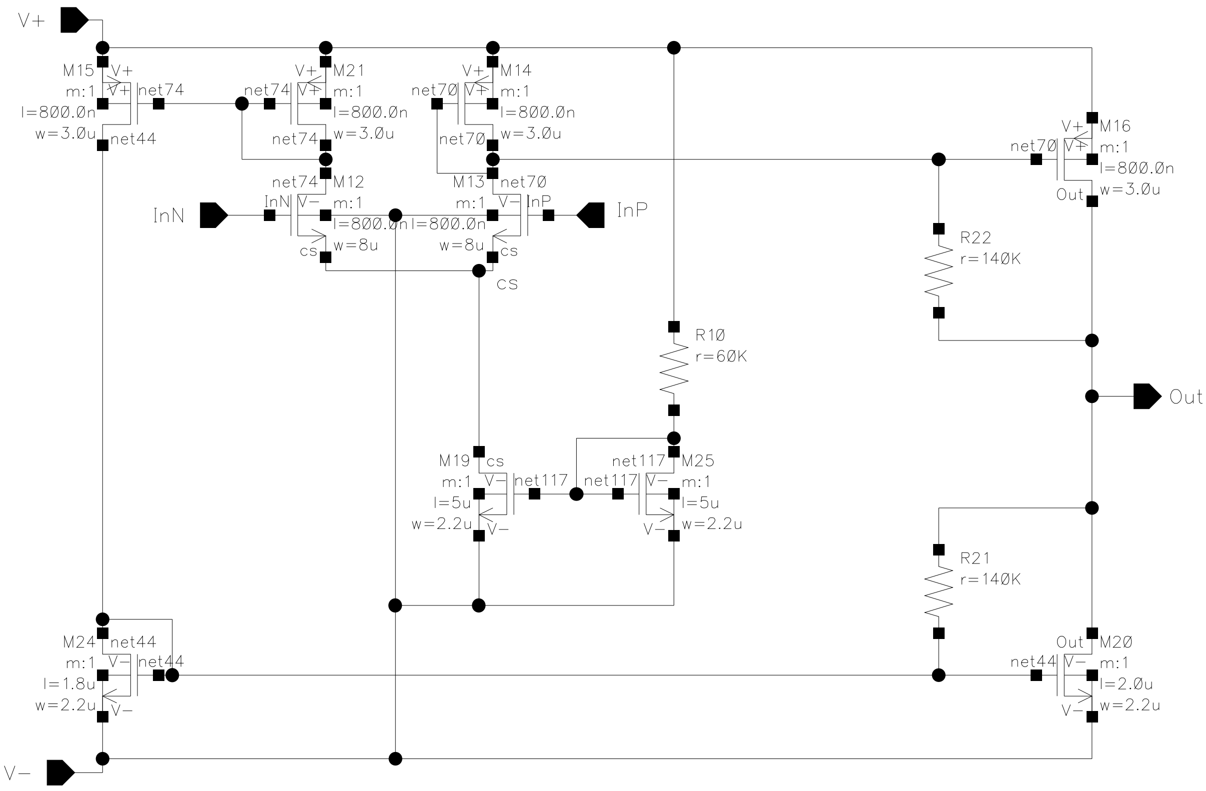
LVDS Receiver



LVDS rcvr schematic : Oct 18 16:32:36 1999

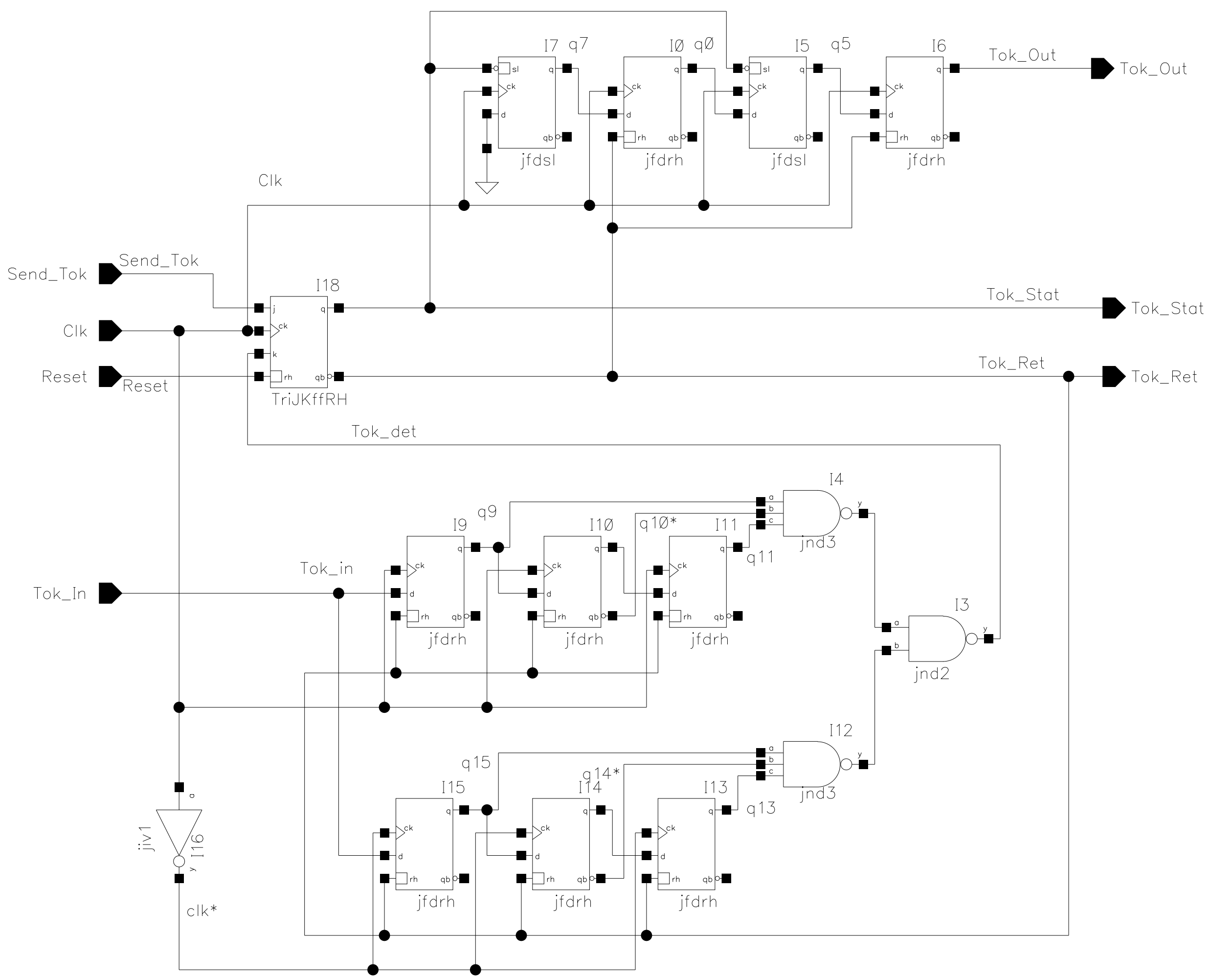


Differential Amplifier



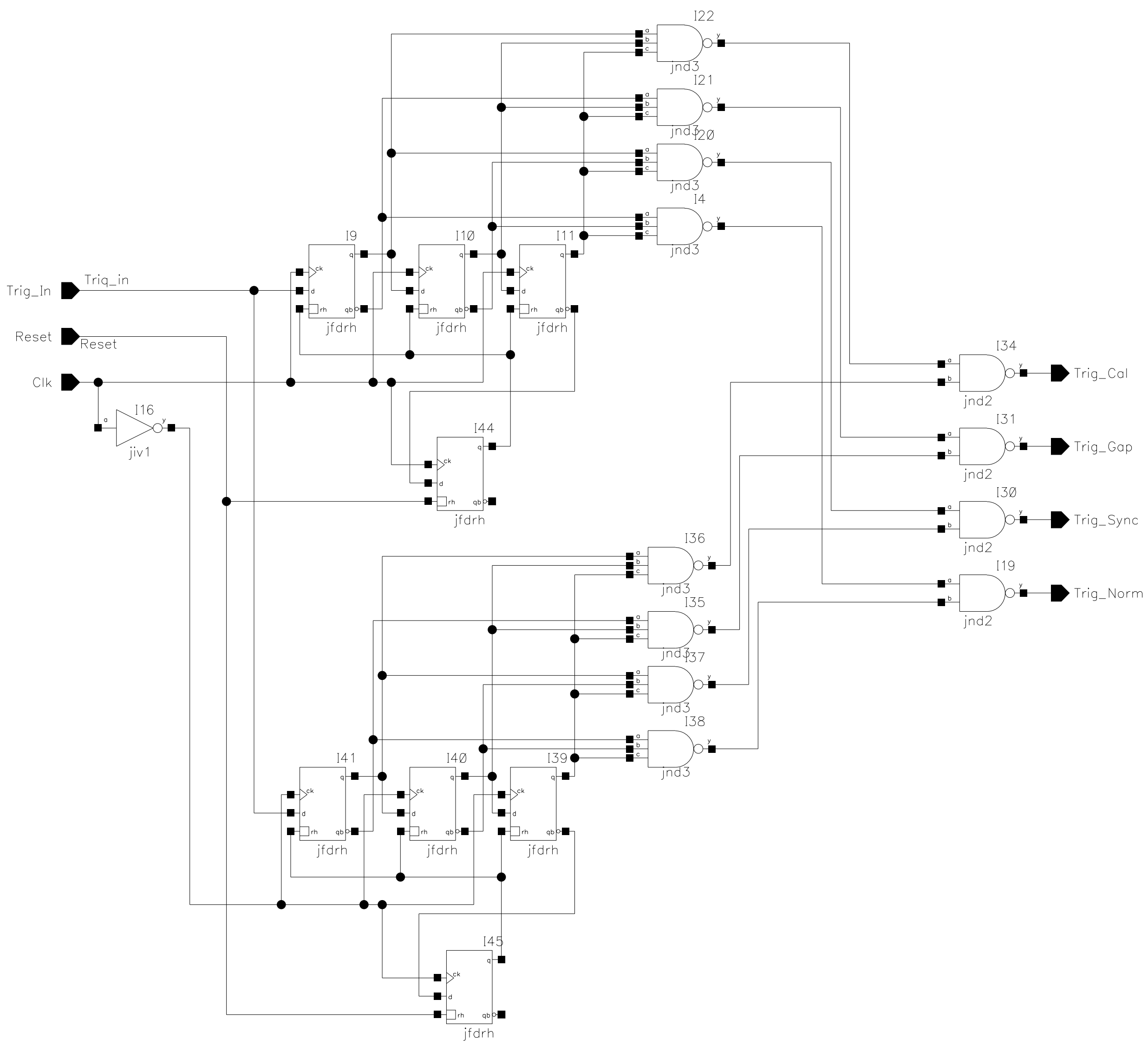
- Gain = 5.5
- f_{3db} = 270 MHz
- t_{rise} = 1.7 ns
- Phase$_{margin}$ = 27^o

Token Control



- Token pass is 101
- allow for uncertainty in phase of incoming token

Trigger Decoder



Schedule

August 99 submitted:

– LVDS driver

November 99 submission:

– LVDS driver (fixed)

– LVDS receiver

– token control block

– parts of stack

February 00 submission:

– all blocks except DAC
submitted both separately
and as an integrated package

Questions/Issues

- Number of clock cycles for header/trailer
- Black/White labels for Header/Trailer
- Calibration
- Stack depth
- Programmable stack maximum
- What should be interrogatable by I^2C
- Double pulse on token pass