$\boxed{\text{Pixel FEC Software}}$

Pixel Readout Workshop

PSI 18-19 March, 2002

FEC Software Functions

Interaction with CNH

—Initialize ROC DAC settings, load pixel trims

—Enable/disable L1, sync, reset triggers

—Enable/disable calibration triggers

—Coordinate refresh of pixel trims

Database access

—Lookup all 30M pixel trims

—Lookup DAC settings for 12K ROC

—Handle data updates during run

Trim refresh rates

— I2C at 40MHz —> 925 ns/pixeltrim
(37 bits at 25ns/bit)

— 2756 pixels x 925 ns = 2.5 ms per ROC
(or 1/30 ROC per 88 μs empty orbit period)

Trim bit and DAC loading

----Data format from FEC to CNH on I2C

Start	Hub add	Port sel.	Start	Addr	R or W	ACK	Data	ACK	Data	ACK	Data	ACK	Stop
1	5bits	3bits	1	7bits	1	1	8bits	1	8bits	1	8bits	1	1

Repeated N-times (37 bits/pixel)

Modular and Hierachical Design

—Barrel, Fdisk

— Multi VME cards

— Multi CNH-Port (sub-VME card)

— CNH level (1 to 8? ROCs per CNH-port)

— ROC level

Sub-CNH function design steps

- Work with Ed on FEC arch. design
- build standalone (multi)chip level function:
  - chip downloading
  - calibration
  - GUI interface
  - Labwindows–VME–Win2000
  - (like Vienna system software)
- add periodic resets, trim refresh
- replace Labwindows interface with SCADA or equiv.
- add database access

User Interface

- **Windows GUI for 1st prototype software**
- **later: Linux with TCL/Tk**
- **ROC threshold, DAC setings**
- **ROC pixel trimming**
- **Occupancy maps**
  - Chip level (individual hot pixels)
  - CNH level (ROCs)
  - Module/Placquette (CNHs)
  - rϕ, z (Barrel)
  - blade, disk (Fpix)