WBS-8 GEM

Requirements:

1. <100 um position resolution (giving better than 1mr angular resolution with 3 GEMs). Achieved 75 um at OLYMPUS.
2. At least 95% efficiency (this has been established with OLYMPUS, and meanwhile also with the GEM telescope at PSI used in test beams at piM1). Can use any-2-of-3 to define track for higher efficiency.
3. No time information; GEMs require external trigger
4. GEM track to provide reference direction for scattering angle measurement
5. Readout speed of 2 kHz at 20% deadtime, corresponding to 100 usec readout time per event

Steps to achieve fast readout:

Currently 1.1 kHz readout rate has been established for one telescope at 100% deadtime, where the readout time per event has been 900 usec. For the goal of 2 kHz at 20% deadtime, it is needed to achieve 100 usec readout time per event, a reduction by a factor 10.

One can gain a factor 2-3, i.e. 500 microsec. by implementing block transfer of 32-bit words. However, another factor 5 is needed.

With the existing system design, one can gain another factor 3 by

using three VME crates with three CPUs and MPD FPGA boards,

respectively, i.e. by adding another two sets. Hampton has one spare VME crate with CPU and MPD from OLYMPUS still available. Reading out with one VME crate per GEM will require a slight reconfiguration of the telescope cabling. The cost for this approach is included in this WBS.

32-bit block transfer is supported by the presently used CPU with the Tundra/universe chipset and by the FPGA (MPD) board. It has been observed that the system with the Tundra/universe chipset performs a factor 4 slower than a comparable system, e.g. based on the tsi148 chipset. We recently purchased a new controller with this chipset, for which also 64-bit block transfer (for another factor 2) is supported by the VME crate and the FPGA (MPD) board. Hence, we expect a factor 8 from this change, which would be sufficient. With this new controller, also the VXS extensions 2eVME and 2eSST are supported by the VME crate and MPD board, which could give further factors, then allowing e.g. multi-frame readout. Using the new CPU requires a re-write of the frontend DAQ software, which has been started.

Alternatively, it has been discussed to avoid the VME bus limitation by employing a UDP protocol via PCI bus. This option will be explored further but requires R&D and hence involves certain risks.

One telescope along with one MPD has been returned from PSI back to Hampton, where one set of VME crate and both CPU types are available. We are also in close contact with the JLab DAQ group for the development of the DAQ system and frontend software.