The CDF Silicon Detectors
Construction, Installation and Commisioning

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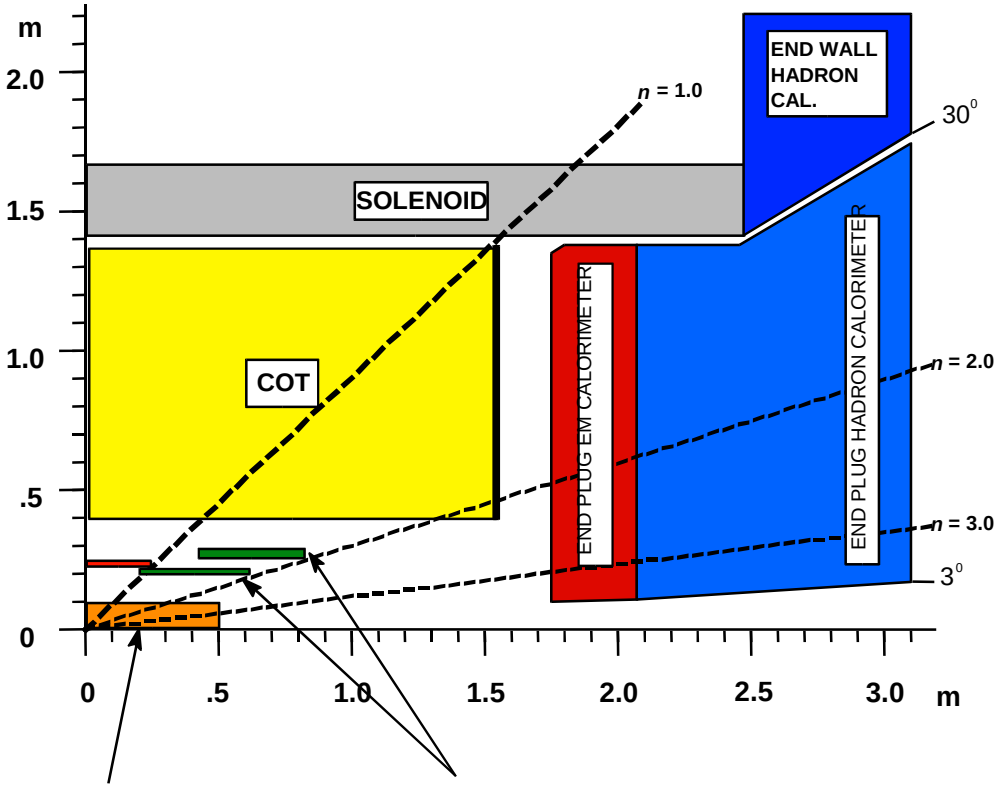
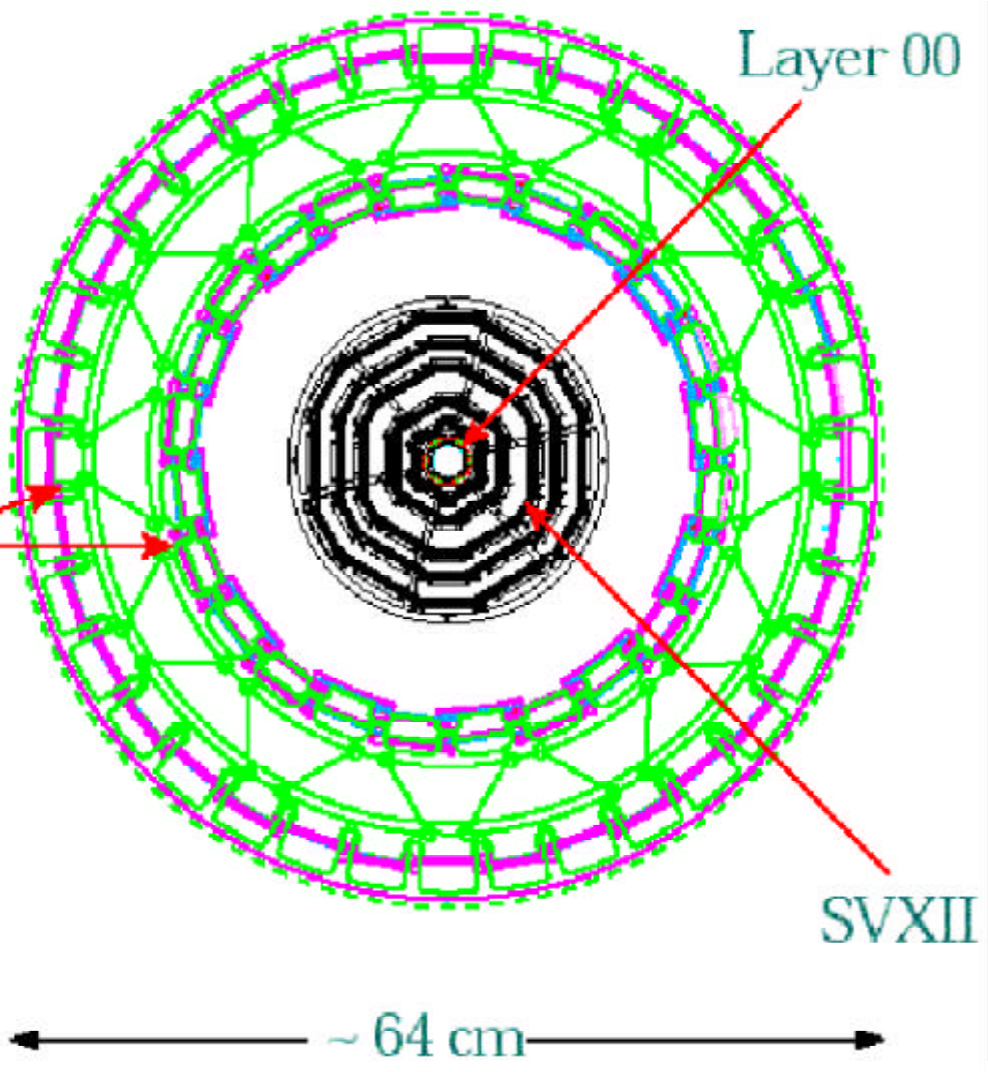
Columbia University, Feb 26, 2002



The rest of CDF...

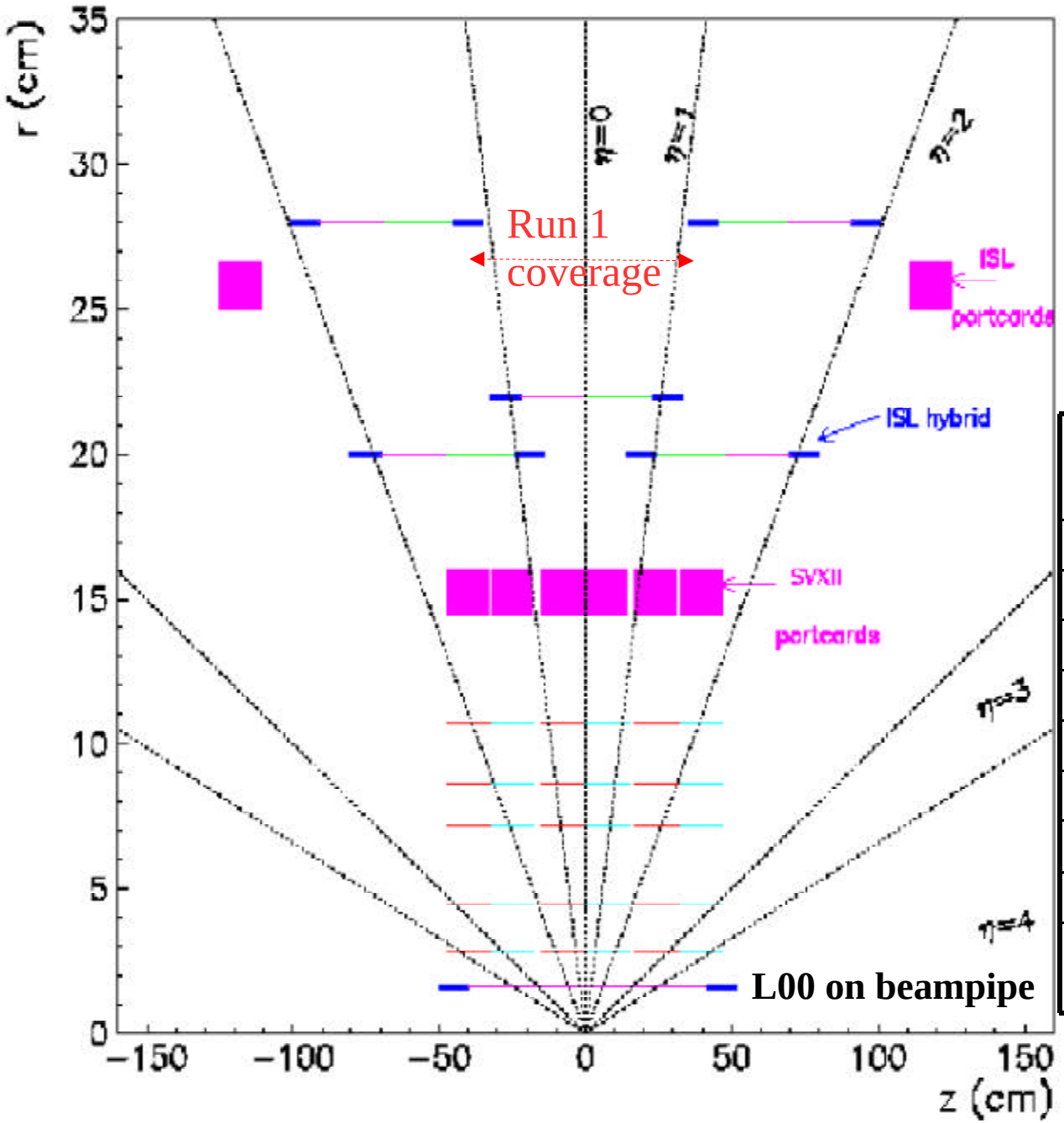
SVX-II

Intermediate Silicon Layer



With 376 modules, 722,432 Readout channels

Silicon detector is 15x larger than in Run1!

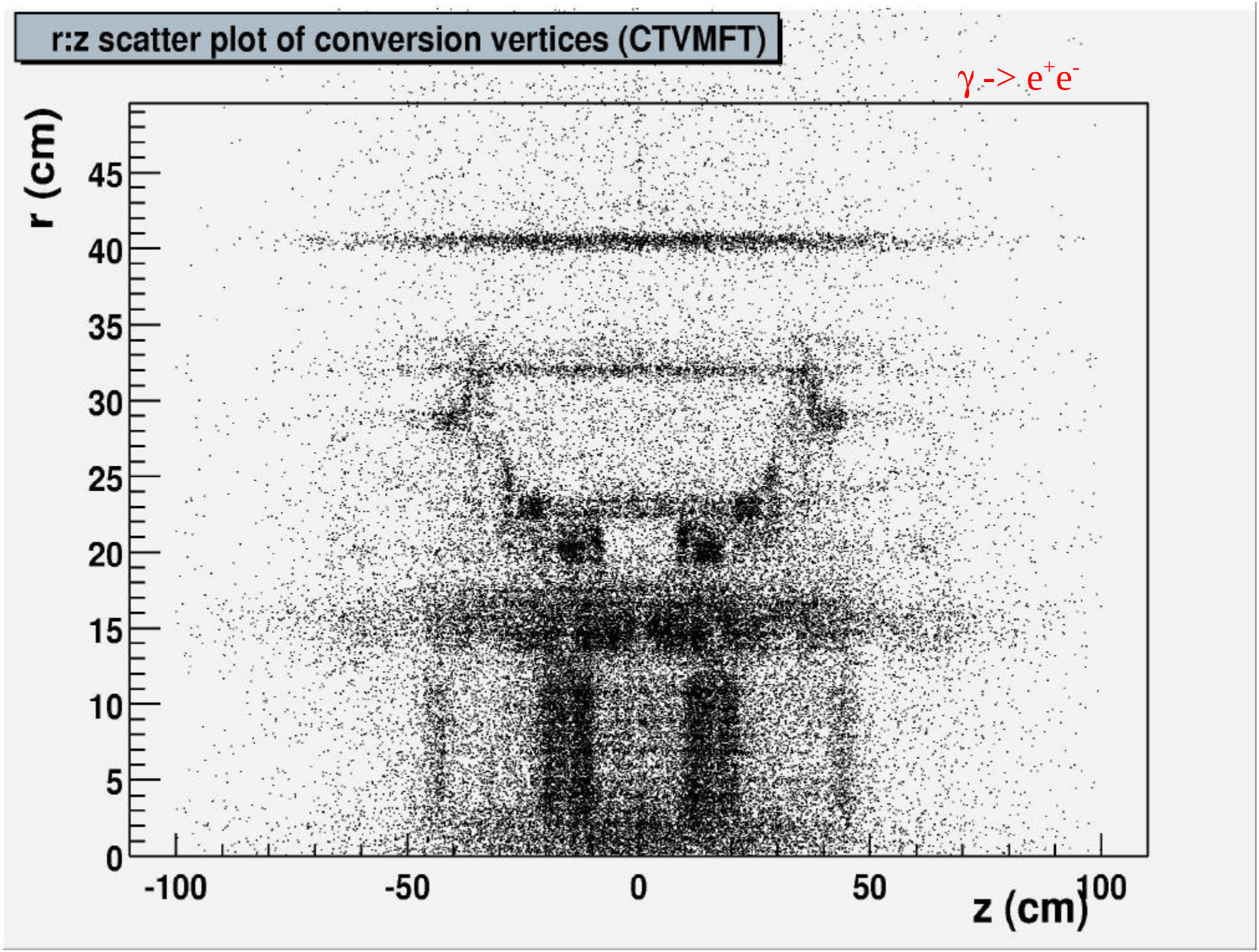


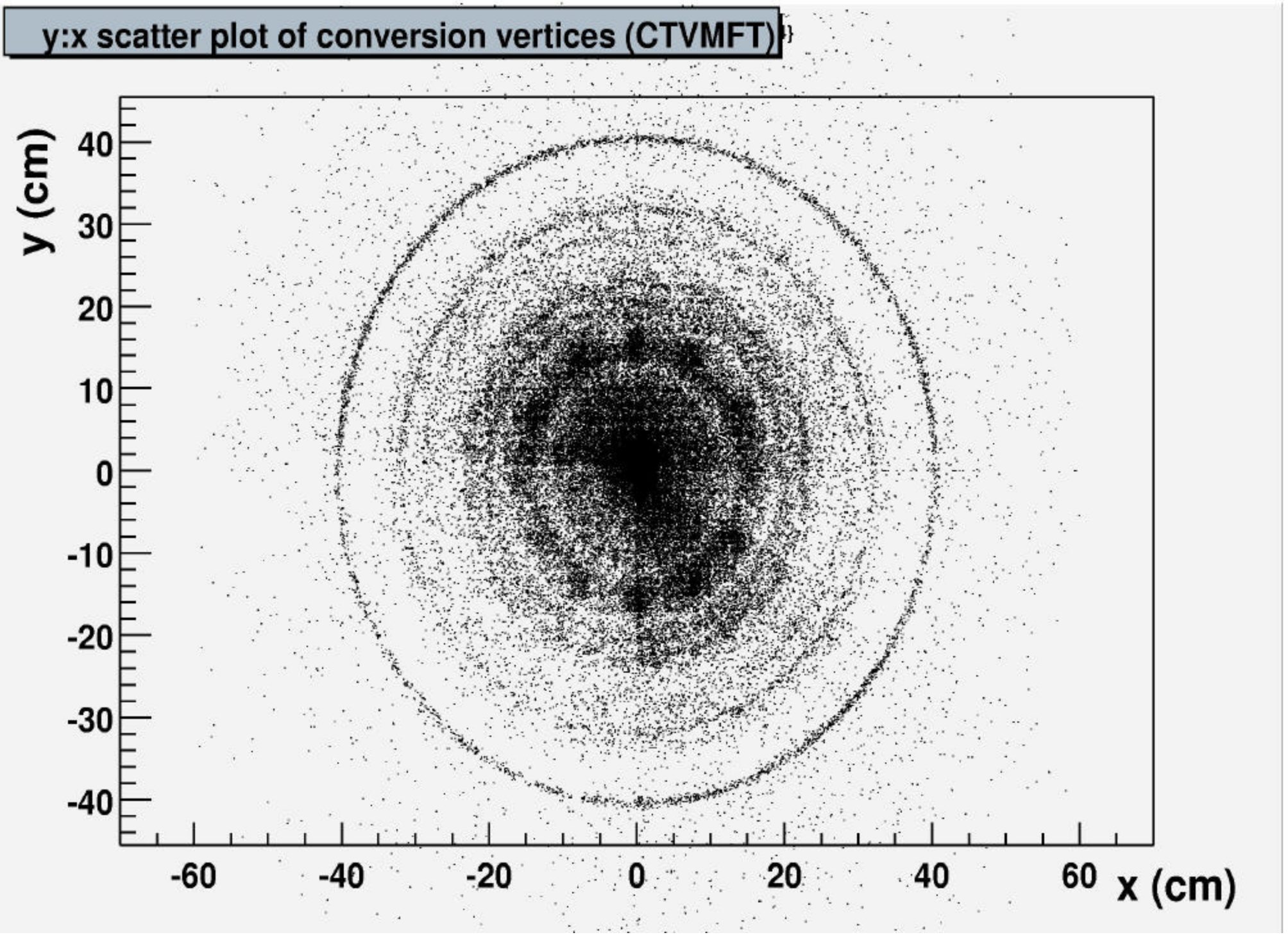
Lots of silicon.

Lots of electronics

Lots of multiple scattering sites.

Layer	Inner/Outer Radii [cm]	Axial Pitch [mm]	Stereo Angle	Stereo Pitch [mm]
00	1.35/1.62	25	-	-
0	2.5/3.0	60	90	141
1	4.1/4.6	62	90	125.5
2	6.5/7.0	60	1.2	60
3	8.2/8.7	60	90	141
4	10.1/10.6	65	1.2	65
5 Forward	19.7/20.2	112	1.2	112
5 Central	22.6/23.1	112	1.2	112
6 Forward	28.6/29.0	112	1.2	112


r:z scatter plot of conversion vertices (CTVMFT)
γ -> e+e-
r (cm)
45
40
35
30
25
20
15
10
5
0
-100
-50
0
50
100
z (cm)

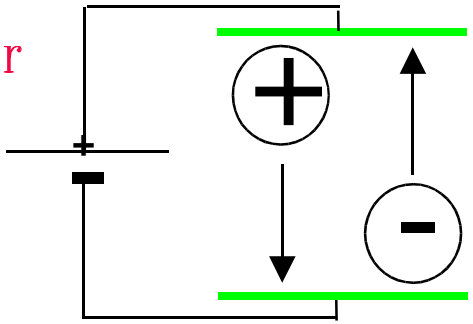

y:x scatter plot of conversion vertices (CTVMFT)
y (cm)
40
30
20
10
0
-10
-20
-30
-40
-60
-40
-20
0
20
40
60
x (cm)

Silicon Detector Basics.

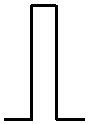
A silicon detector is a ionization chamber

Sensitive volume with electric field

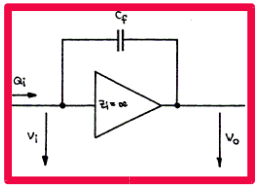
Energy deposited creates e^-–h pairs



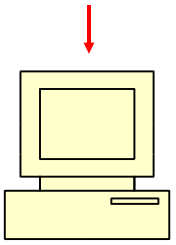
charge drifts



Gets integrated

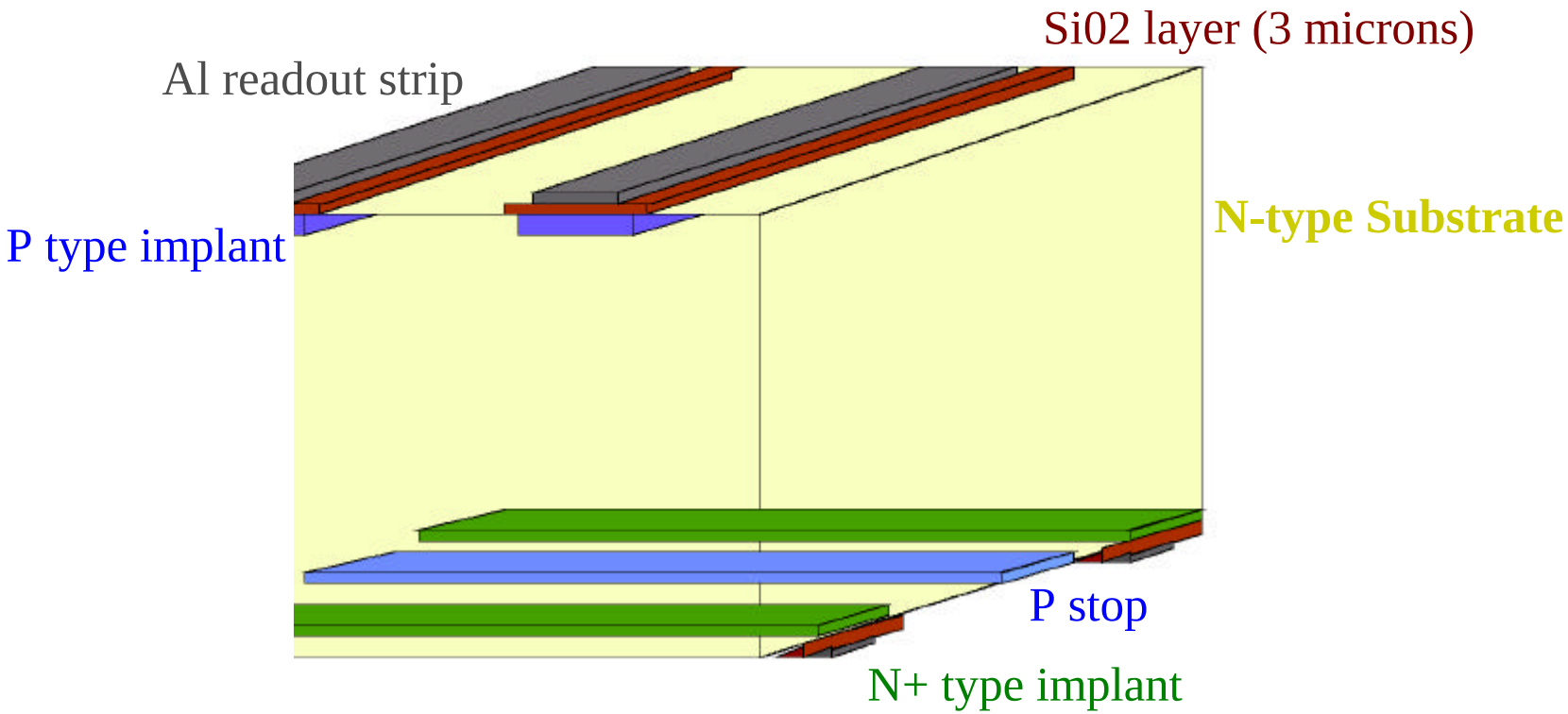


Then digitized

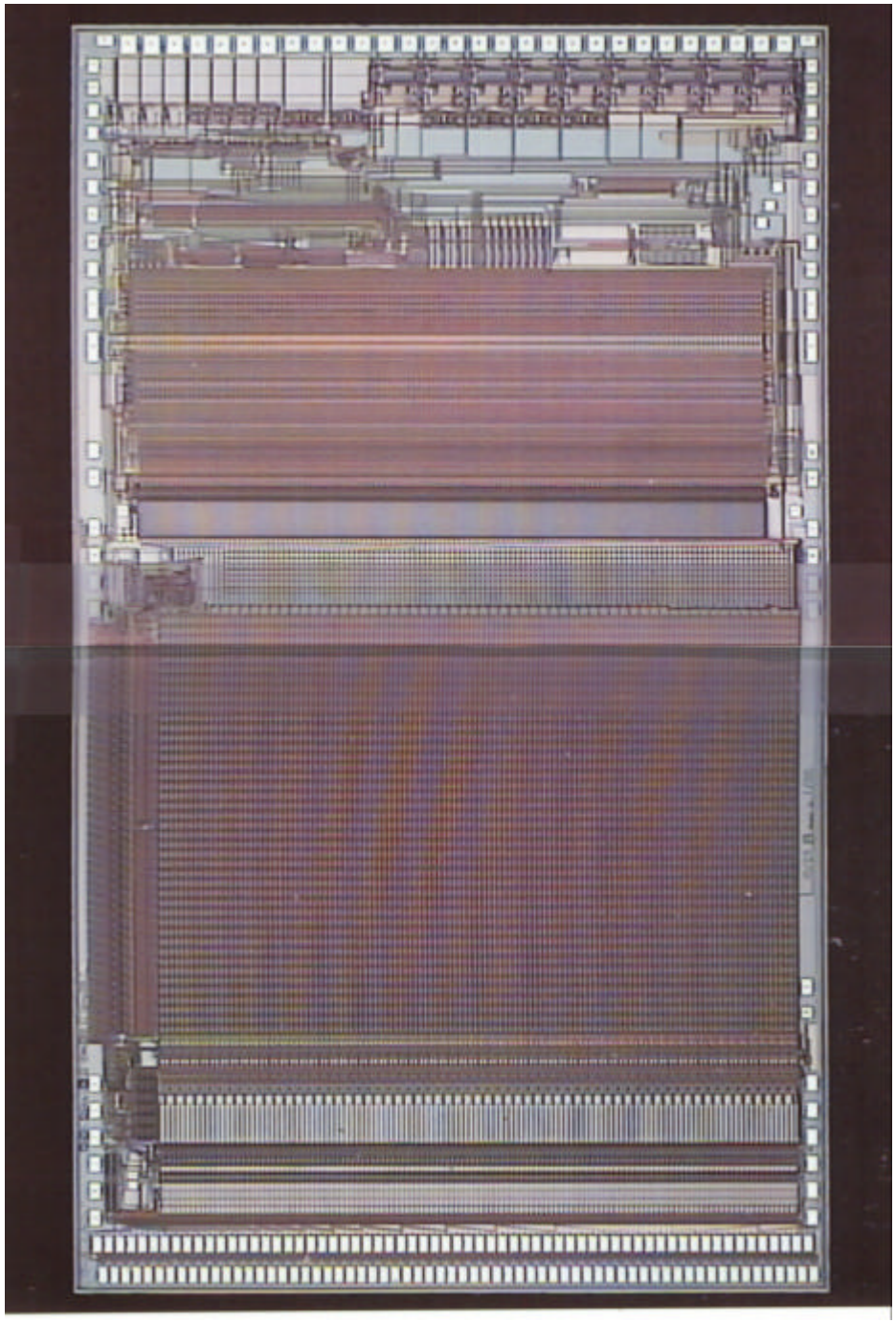


And finally readout and stored

Double Sided Silicon. Readout on both sides



The SVX3 Chip (not to scale)



Bonding pads to hybrid.

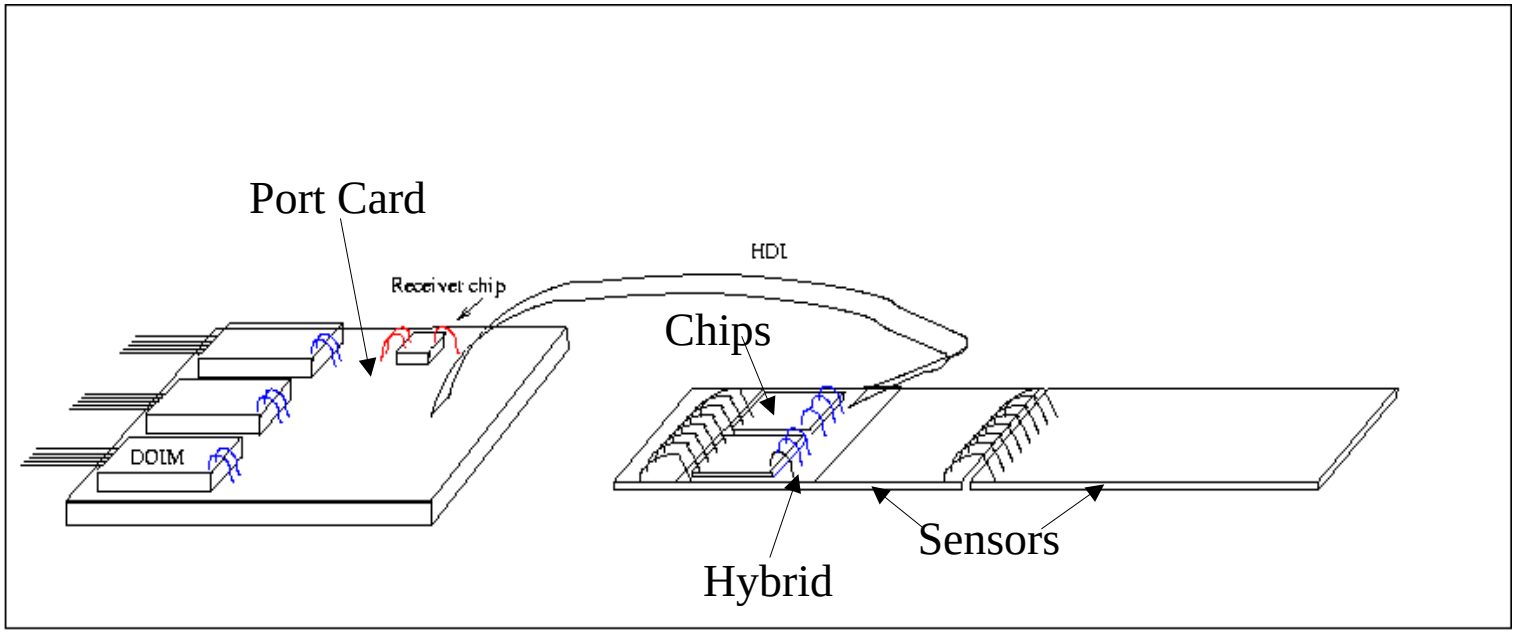
- Analog Front End (FE) and Digital Back End (BE)
  - FE has relatively low noise integrator and 42 cell analog pipeline with 4 buffer cells
  - BE has comparator, ADC, and sparse readout
- **Deadtimeless:**
  - Capable of analog operations during digitization and readout
- **Dynamic pedestal subtraction** (DPS
  - Enables common mode noise suppression

Analog pipeline
42 pipeline cells,
one per 128 channels

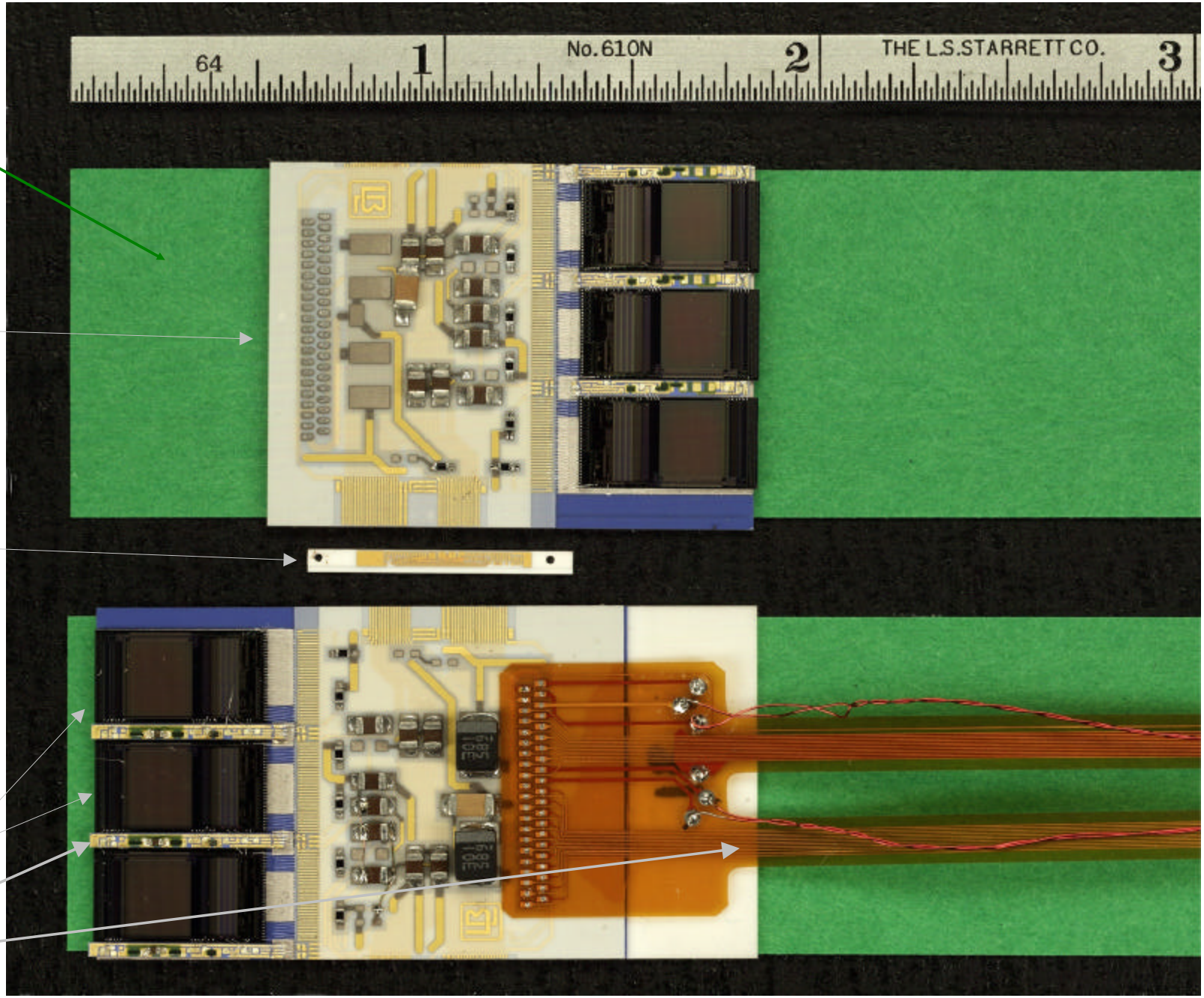
Bonding pads to silicon sensor

Lots of wirebonds hold the system together.

- Chip critical bonds: 310400 (chip wire bonds)
- Ladder (module) critical bonds: 10416 (bias lines, control lines, optical links)
- Wedge-critical: 816 (control lines)
- Non critical bonds (single channels): 1748000 (strips)



Sensor, Hybrid, Chip Layout



"Sensor"

Z side

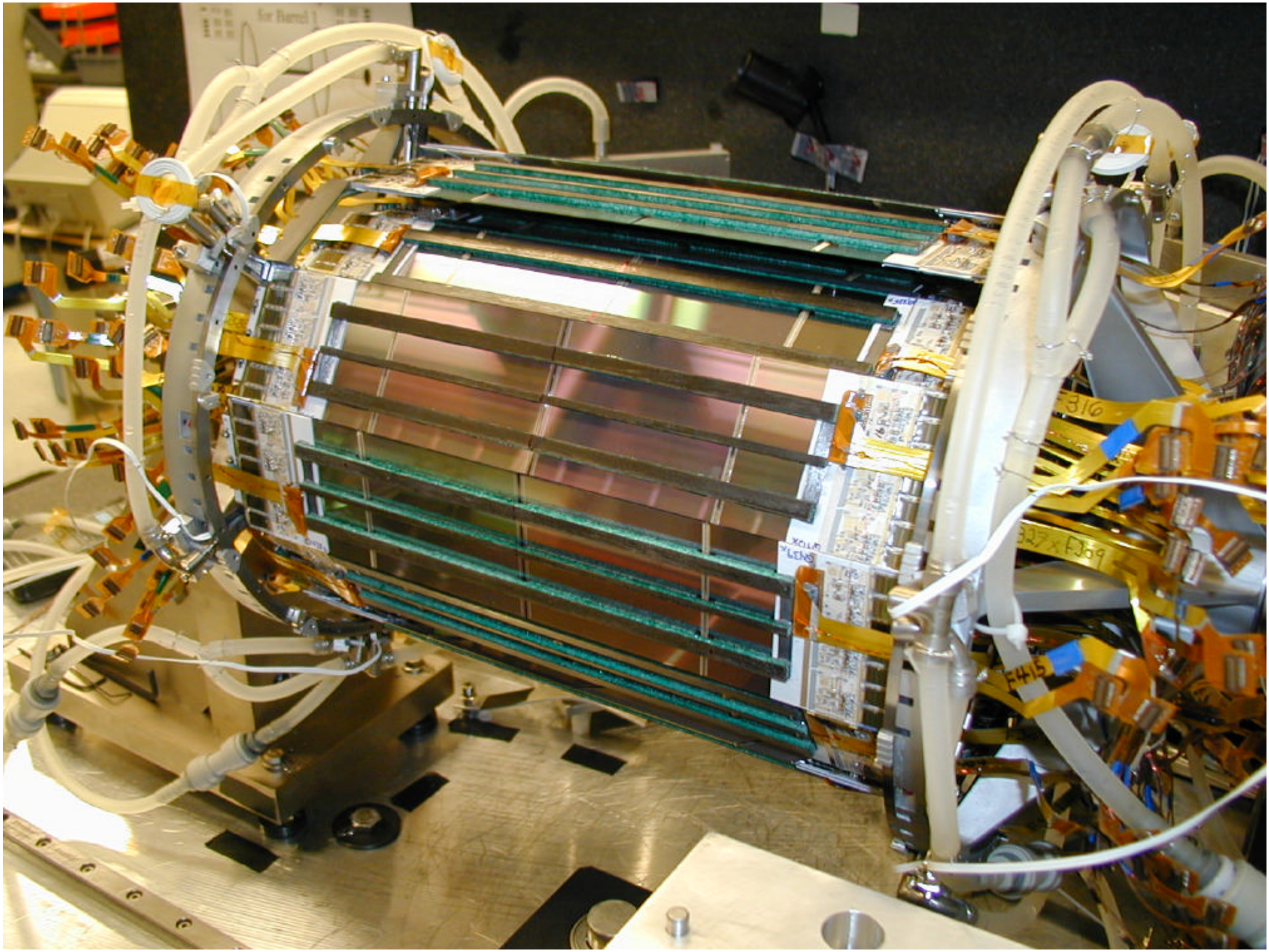
Jumper

Phi side

Chips

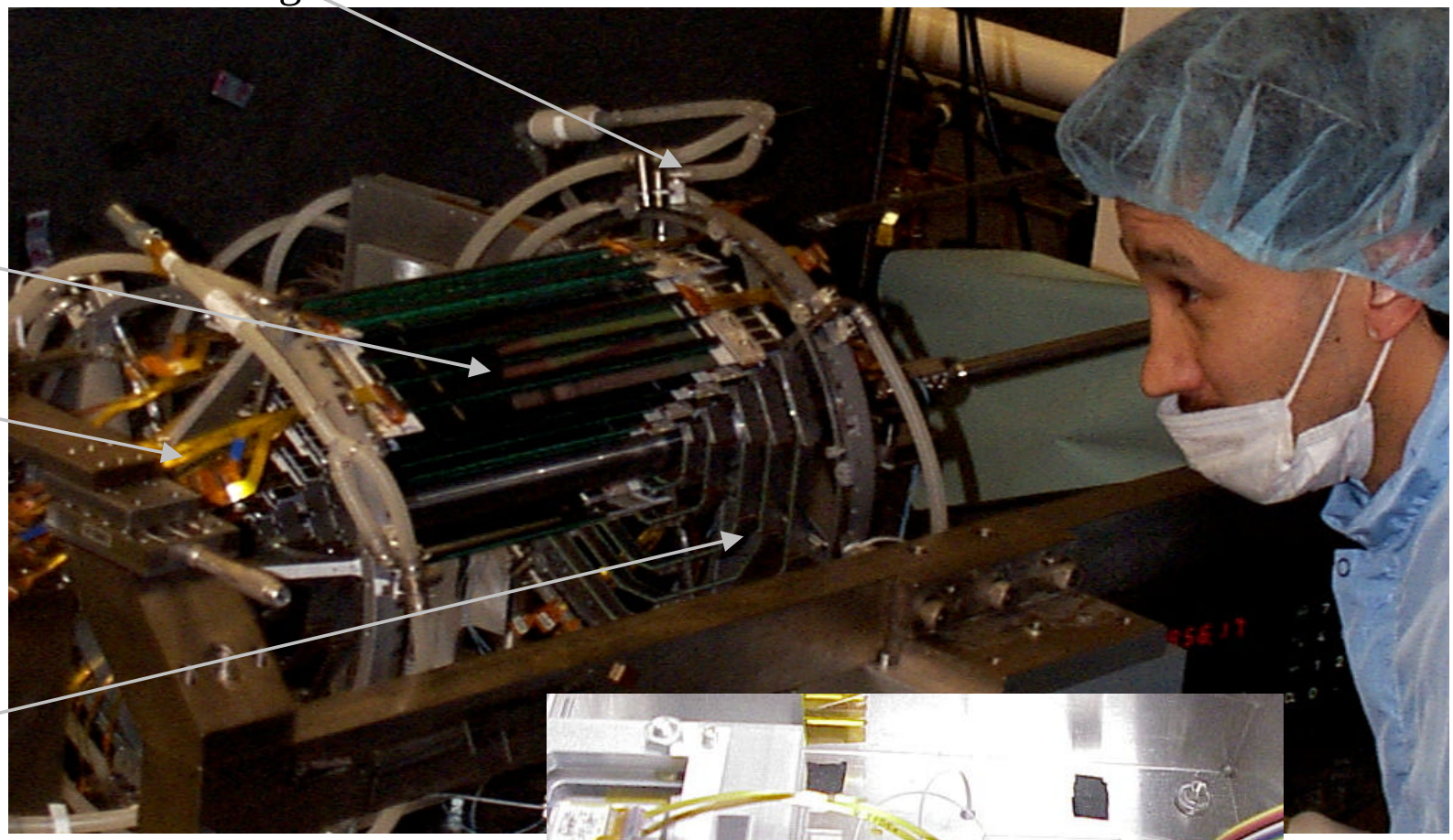
fingers

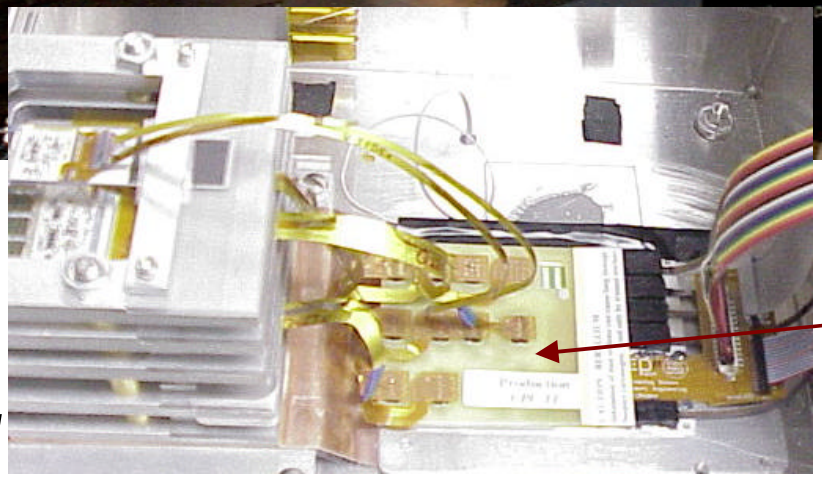
HDIs



Wedge structure for SVX: asking for trouble?

Bert Gonzalez



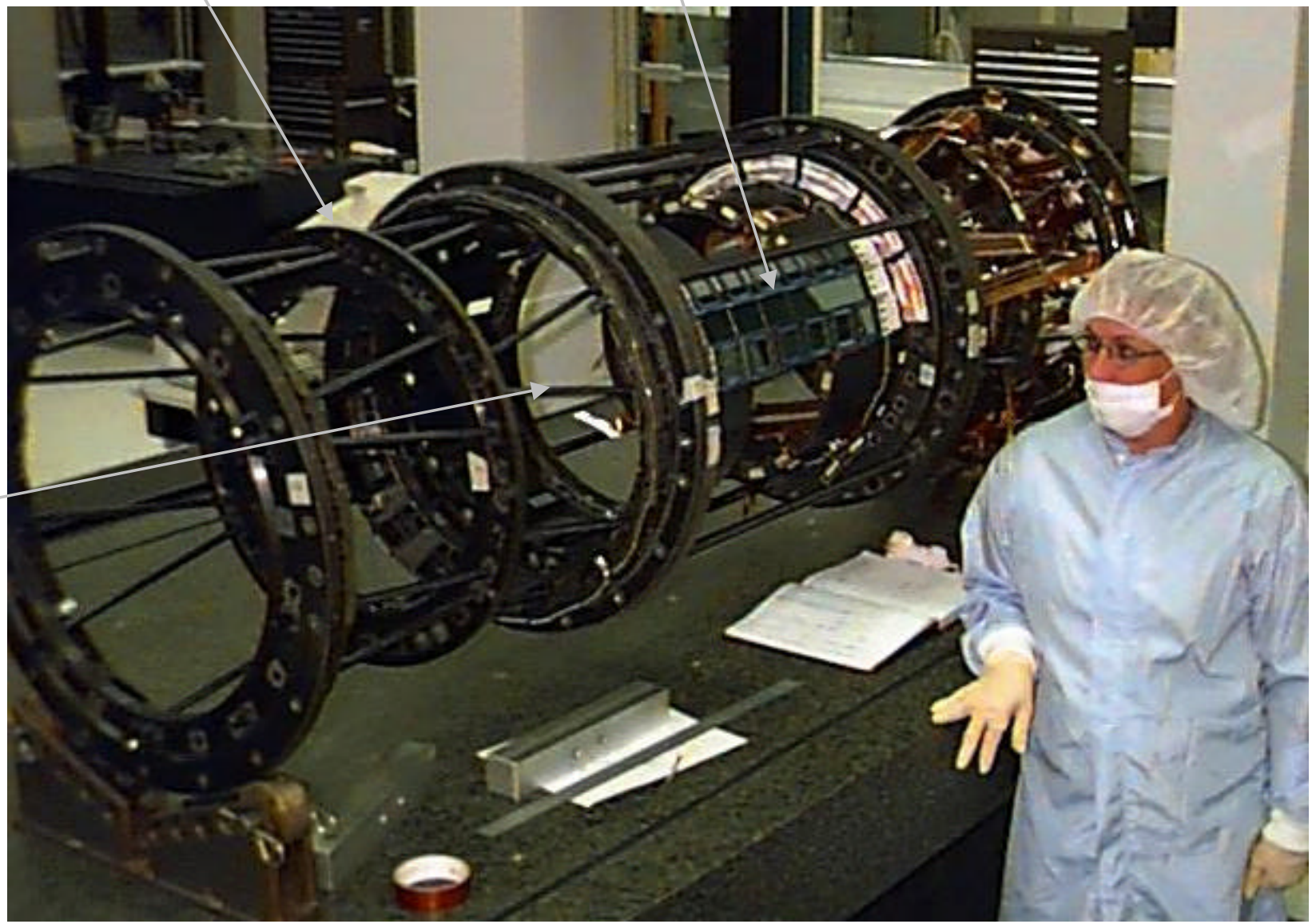


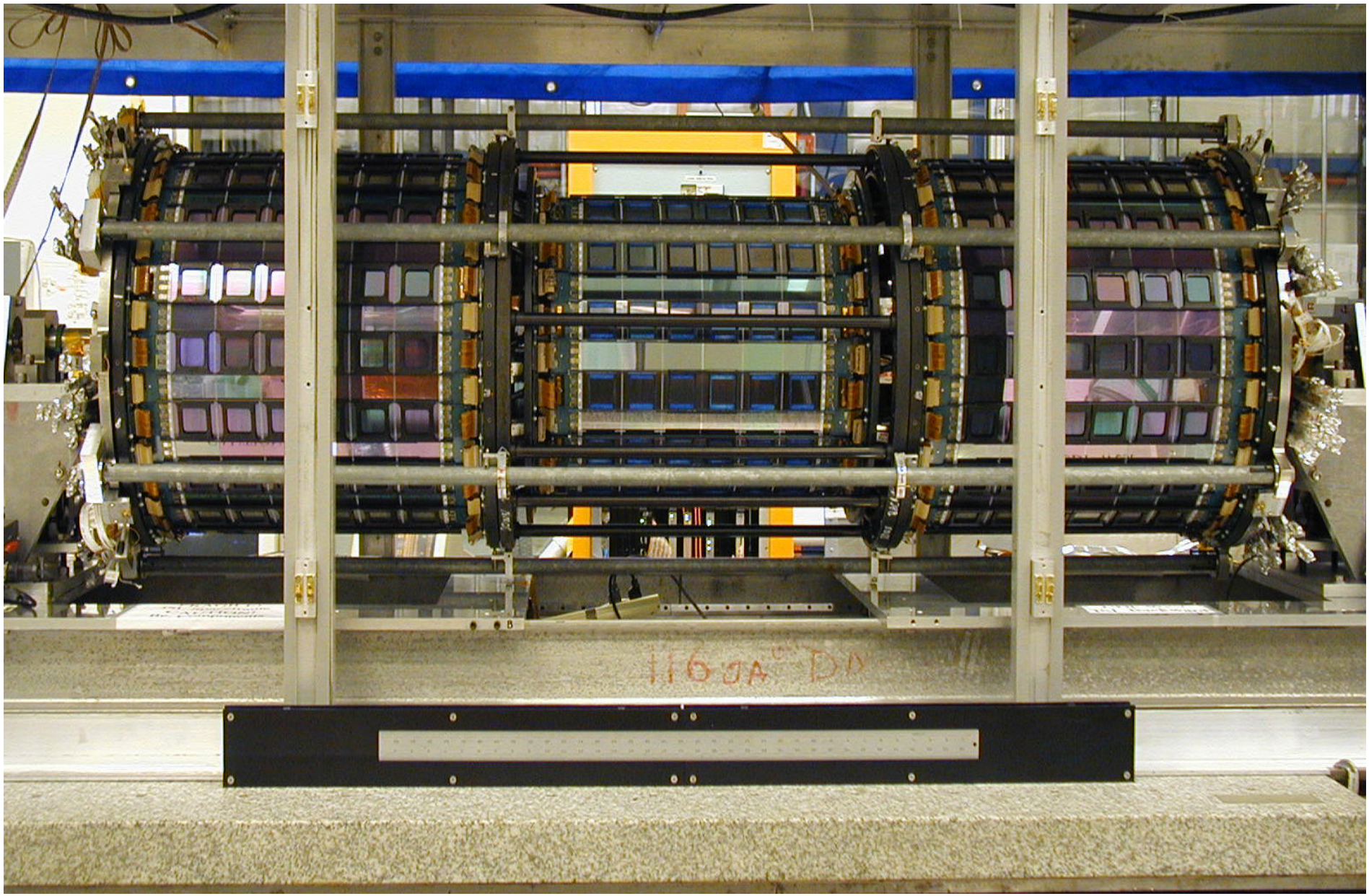
"Wedge in a box"

ISL Carbon-Fiber Frame

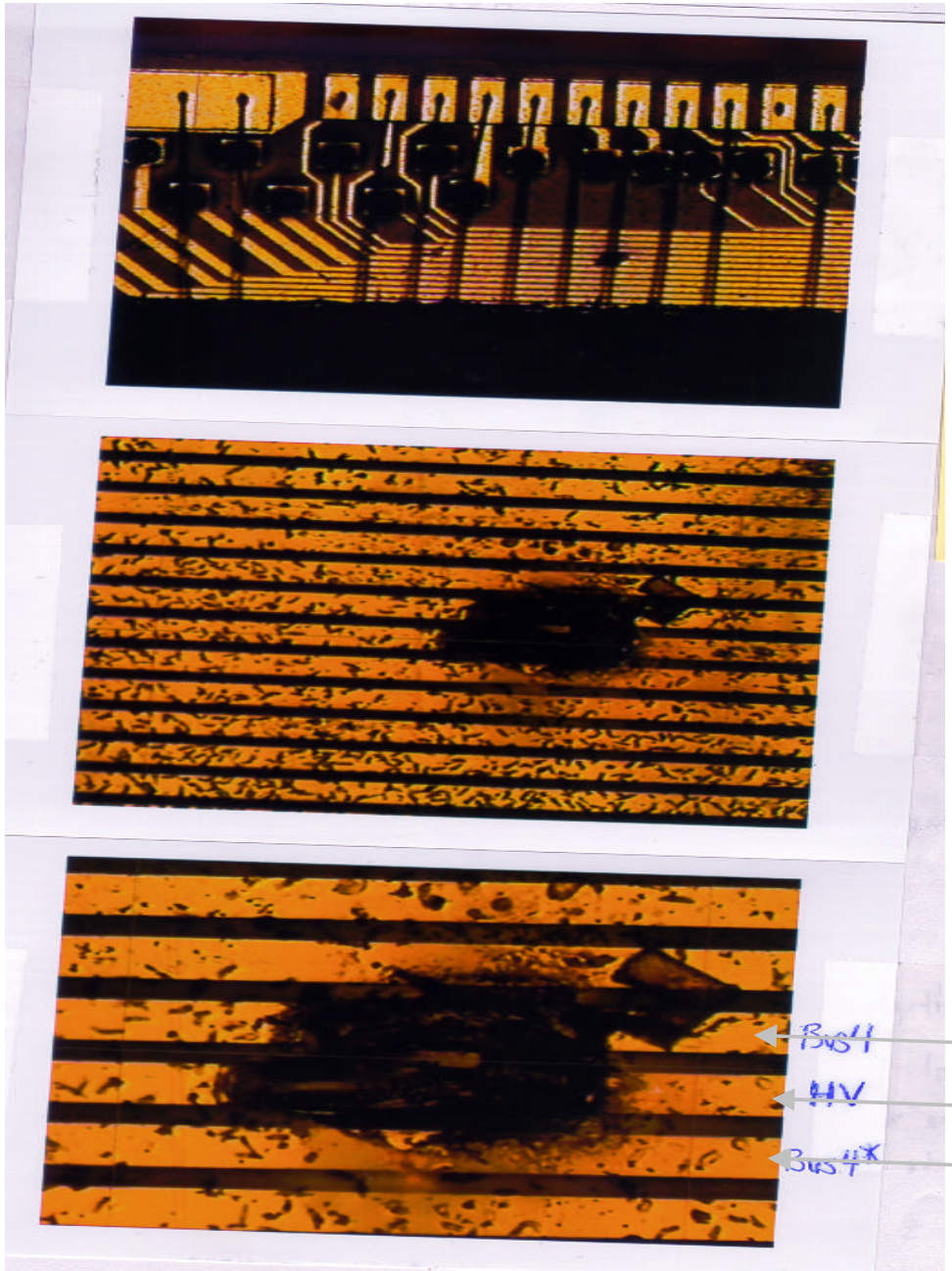
ISL Ladders

SVX goes in here



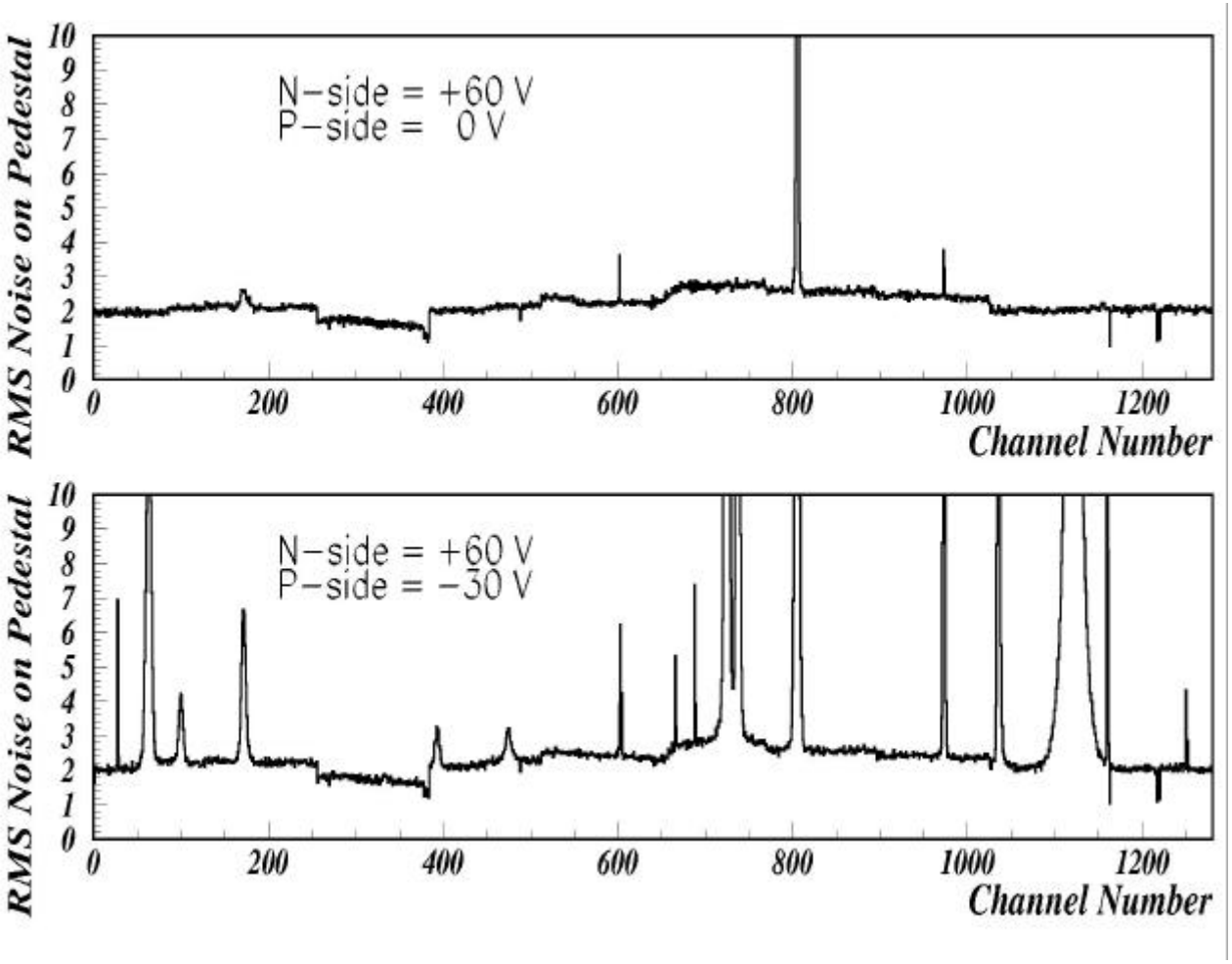

116 JA° DN

Problems found in Production: jumper HV



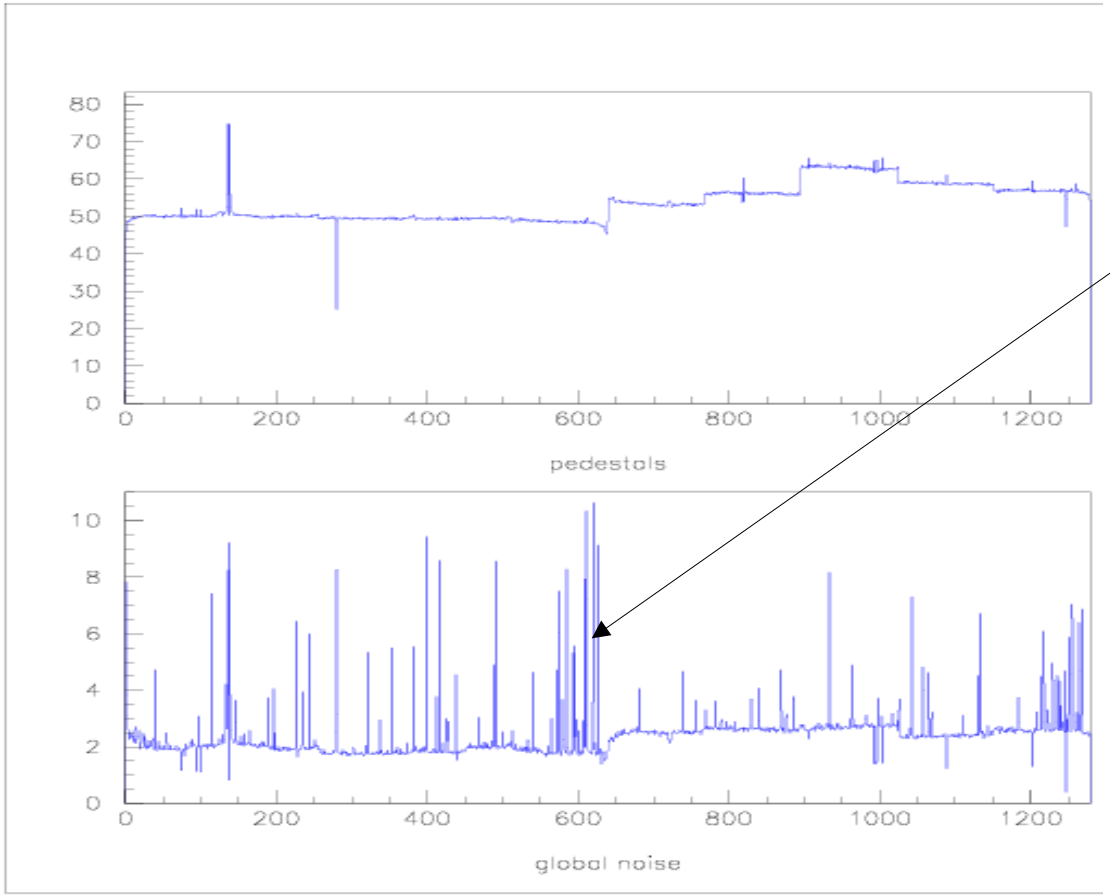
- Jumper did not hold high voltage.
  - Takes signal, HV from phi side to Z side
  - signal/ground traces close to HV traces
- Took **~20 hrs** to blow!
- Solution: copper wire.
- **MORAL: Don't trust electronic design features. Small is different.**

Problems found in production: Micron sensors



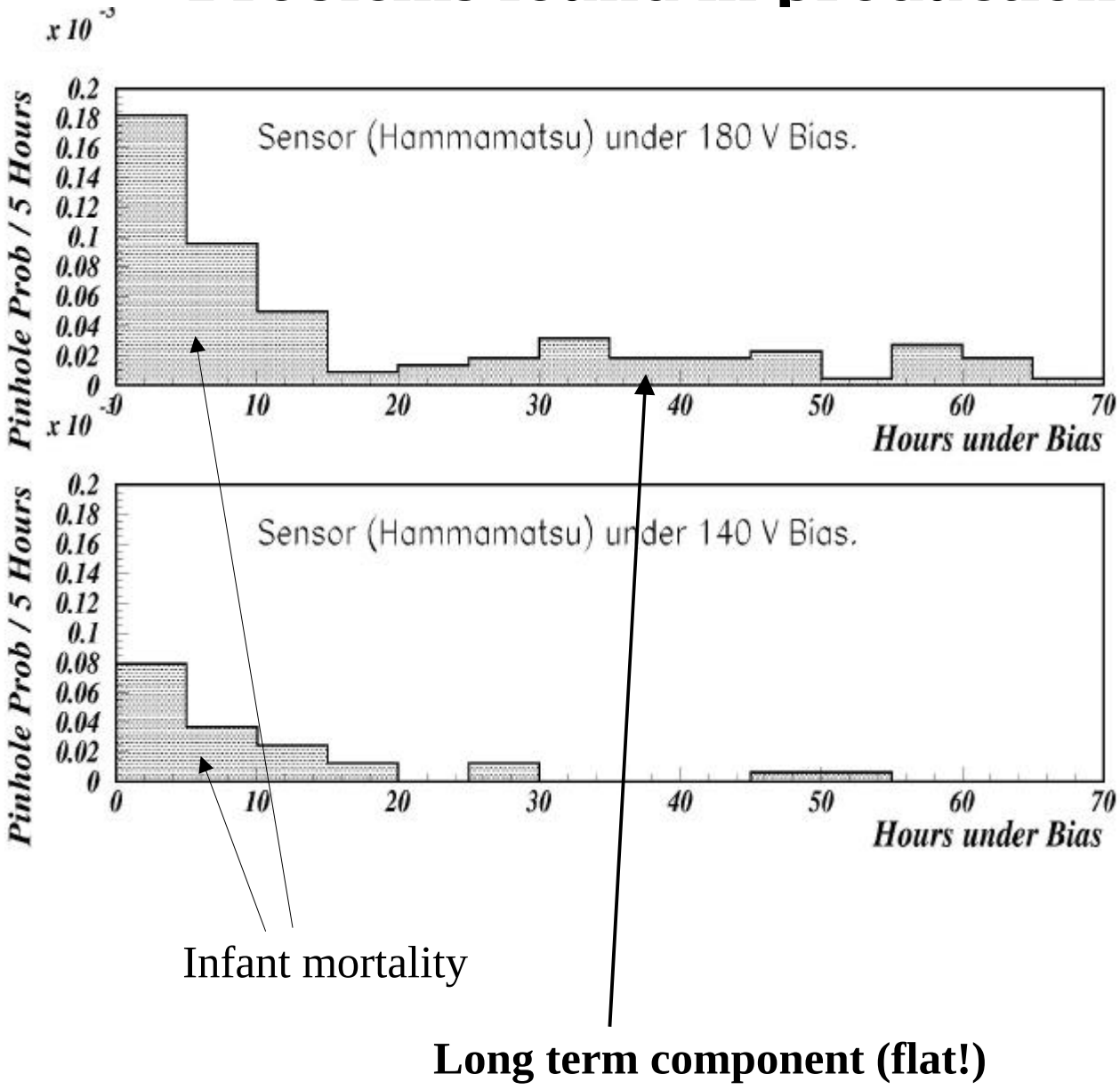
- Micron Sensor (for SVX) could not be biased on both sides
  - Usual depletion bias scheme calls for +Vbias/2 on N-side, and -Vbias/2 on P-side.
- With neg. bias, noise erupted like acne on a teenager.
  - Similar to D0 noise problems.
- Solution: do not neg bias (reduces projected lifetime).
- **MORAL: Keep close watch on silicon vendor's QC .**

Problems found in production: Micron sensors:



- Micron Sensor developed "grassiness".
  - Affected 11 out of 360 ladders.
- Ladders still ok for physics, but with reduced S/N.
- Origin is buildup of oxide charge.
- **MORAL: Keep close watch on silicon vendor's QC .**

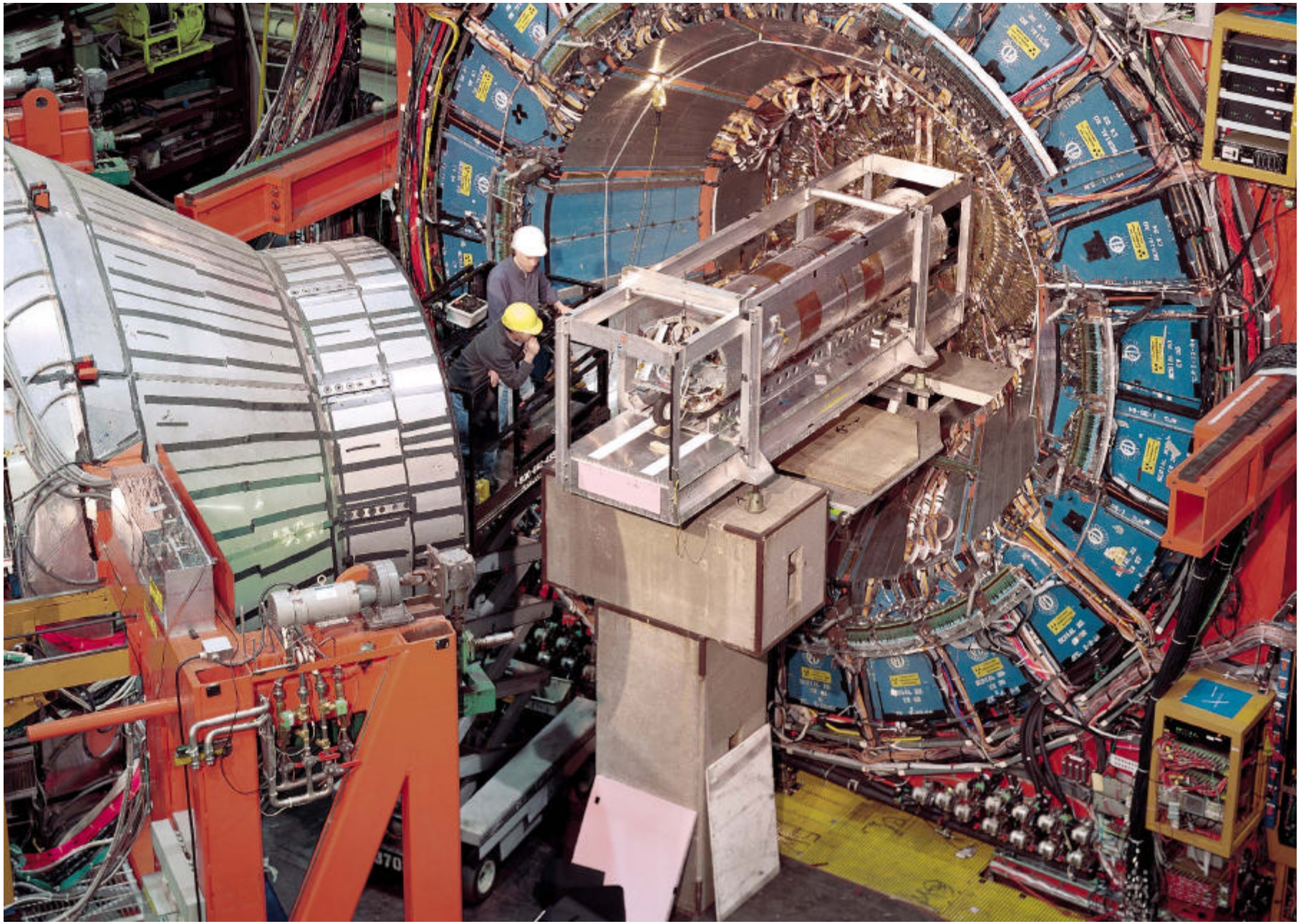
Problems found in production: Hammamatsu silicon



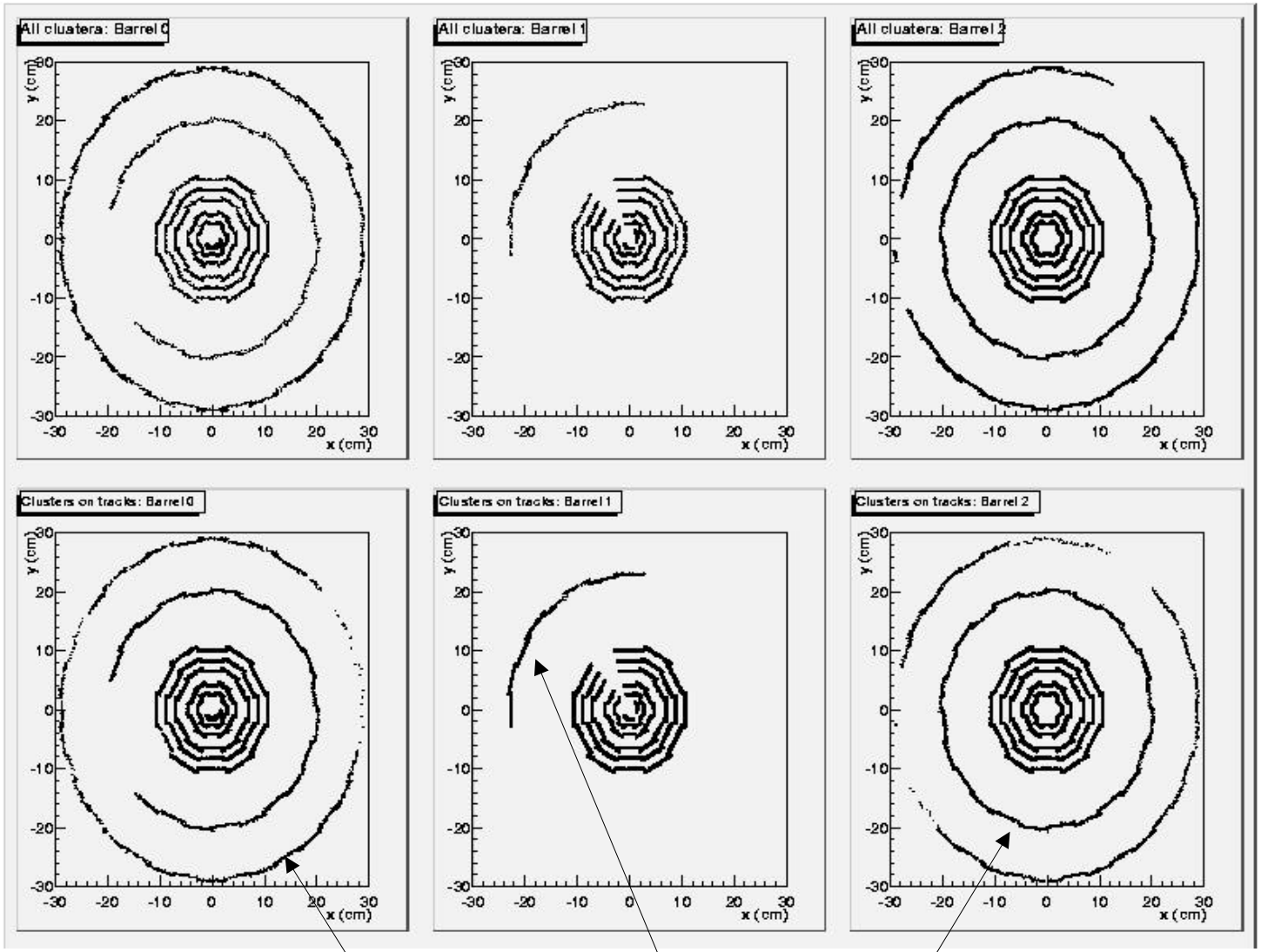
- Hammamatsu sensors rated for ~200 V (100V/side).
  - Sensors have bias capacitors built into design.
  - 3 microns of Si02 b/wn silicon and readout strip.
- During burn-in, we found Hammamatsu sensors produced "pinholes" (single-channel capacitor breakdown) beyond "infant mortality" rate.
- Solution: Can't crank bias to desired level, reduce projected lifetime.
- **Moral: Don't trust vendor specs. Test.**

Silicon Installation

Silicon Installation



Problems found after Installation: ISL Central Cooling

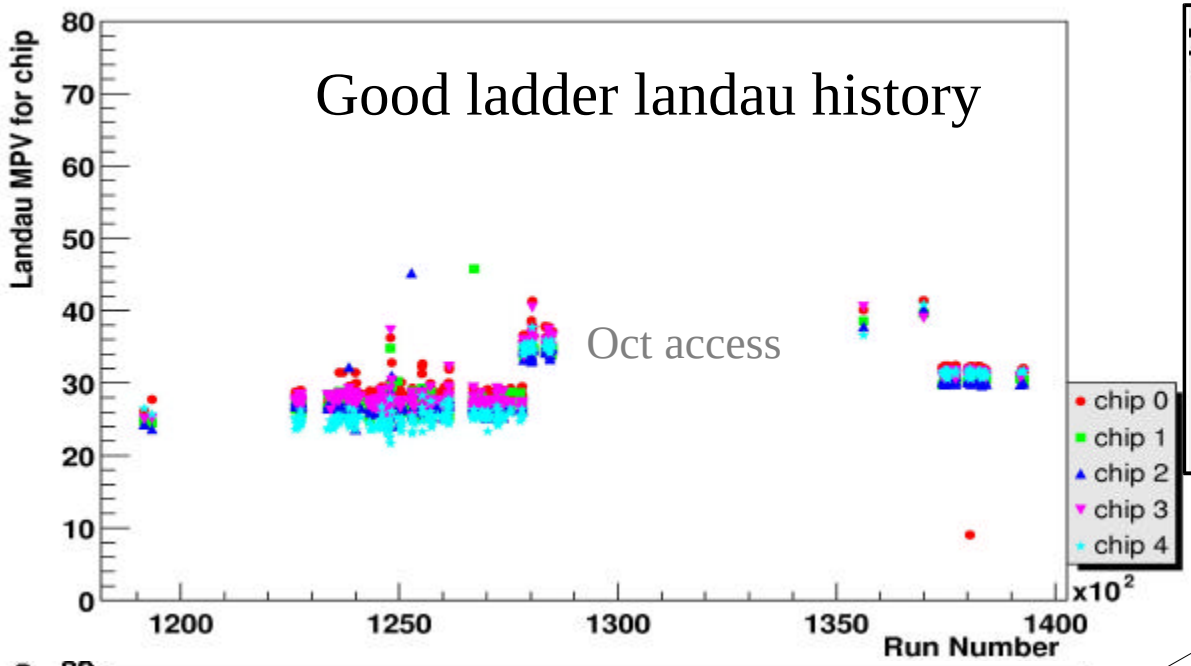


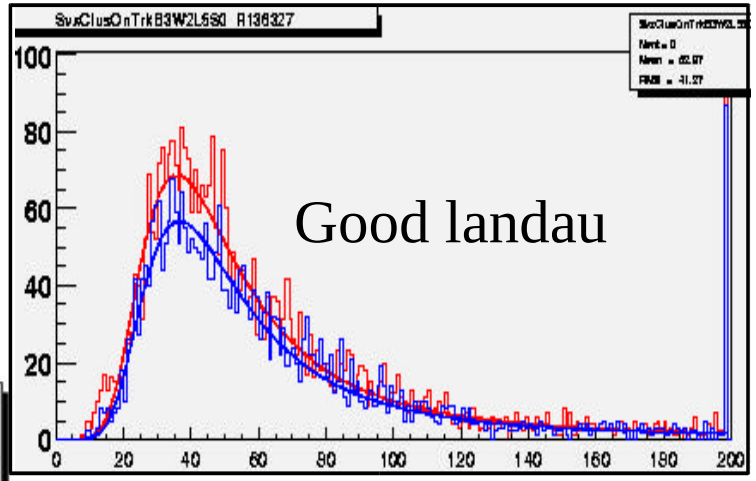
Central ISL off
(recovered ladders on)

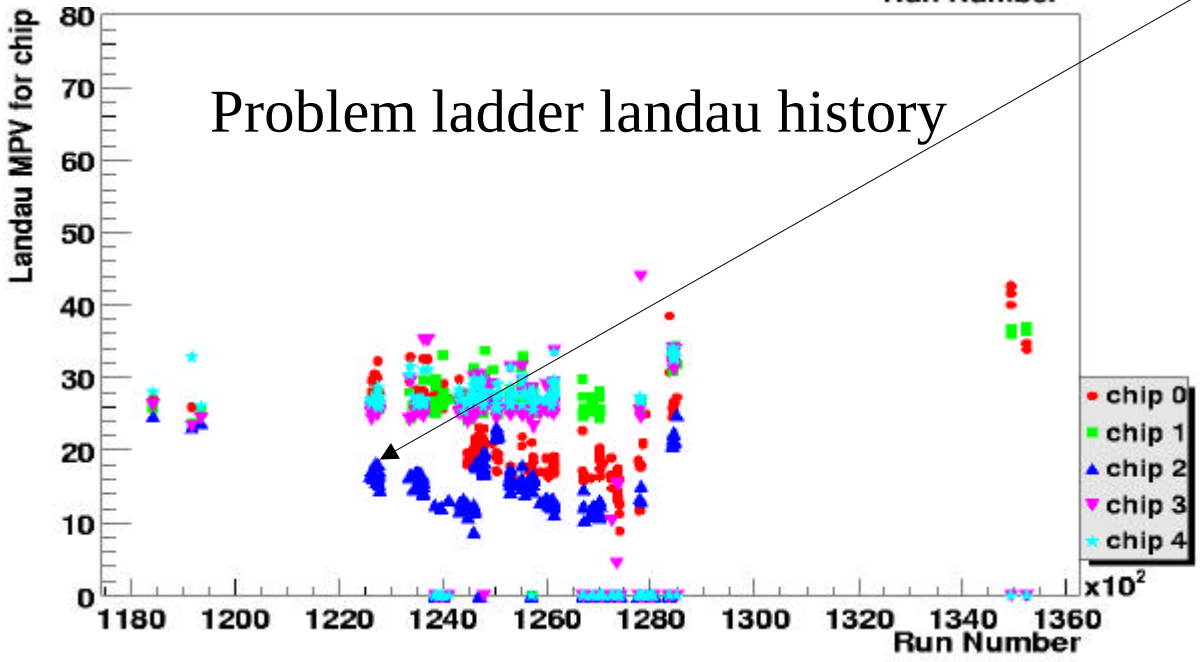
East, West ISL ok.

- ISL cooling system has epoxy blocks.
  - Central ISL cannot be turned on.
- Solution: Surgery. Laser, fiberoptics (and prisms to shoot around corners).
  - Works! One line roto-rootered, recovered.
- **Moral: Full system tests.**

Problems found after Installation: AVDD2 problem





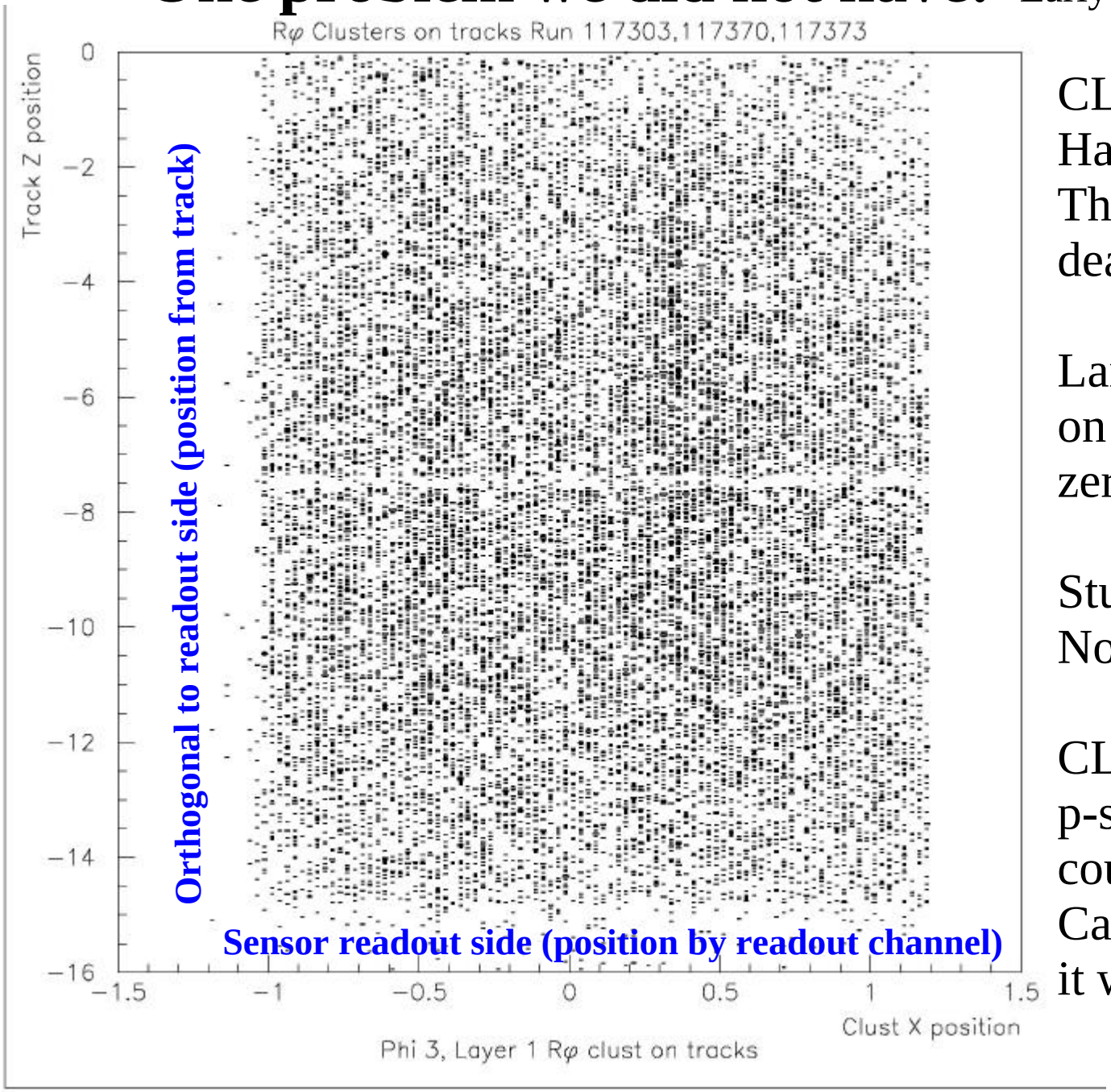


- Chip failure (3rd chip shown). Takes out all chips downstream.
  - Silver epoxy joint on "finger" suspected.
  - Small number of ladders affected.
- Solution: Reduce power, thermal cycling
- **Moral: Torture tests before installation.**

Other Problems: Back-End state

- Front End (analog) of chip sees charge buildup from Back End (digital).
  - Pedestal, noise for ADC can be depend on digitizer state: acquire, digitize, readout, etc. (See separate plot).
  - Can tag state by "time since L1 accept" which is part of readout.
- Solution: Calibration tables x4 for different back end state.
  - Database people don't like us much. (700k chans: ped, noise, dnoise x4).
- **Moral: Isolate analog and digital parts.**

One problem we did not have: Early Sensor Death like CLEO



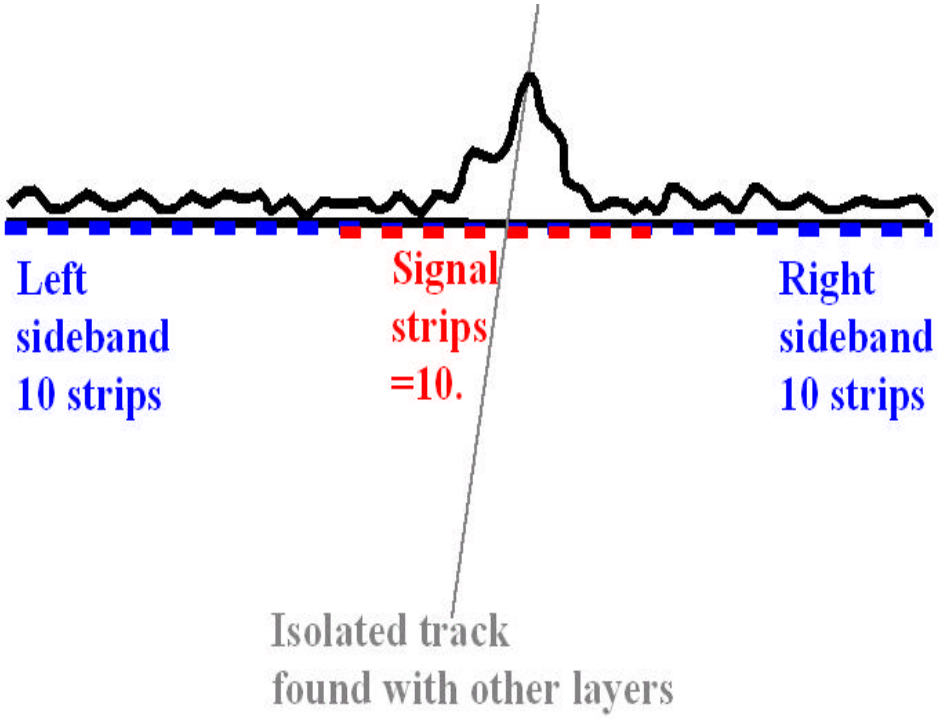
CLEO also used Hammamatsu sensors. They saw early sensor death (few krad!).

Large circular patches on their sensors had zero efficiency.

Studied early at CDF. Not a problem.

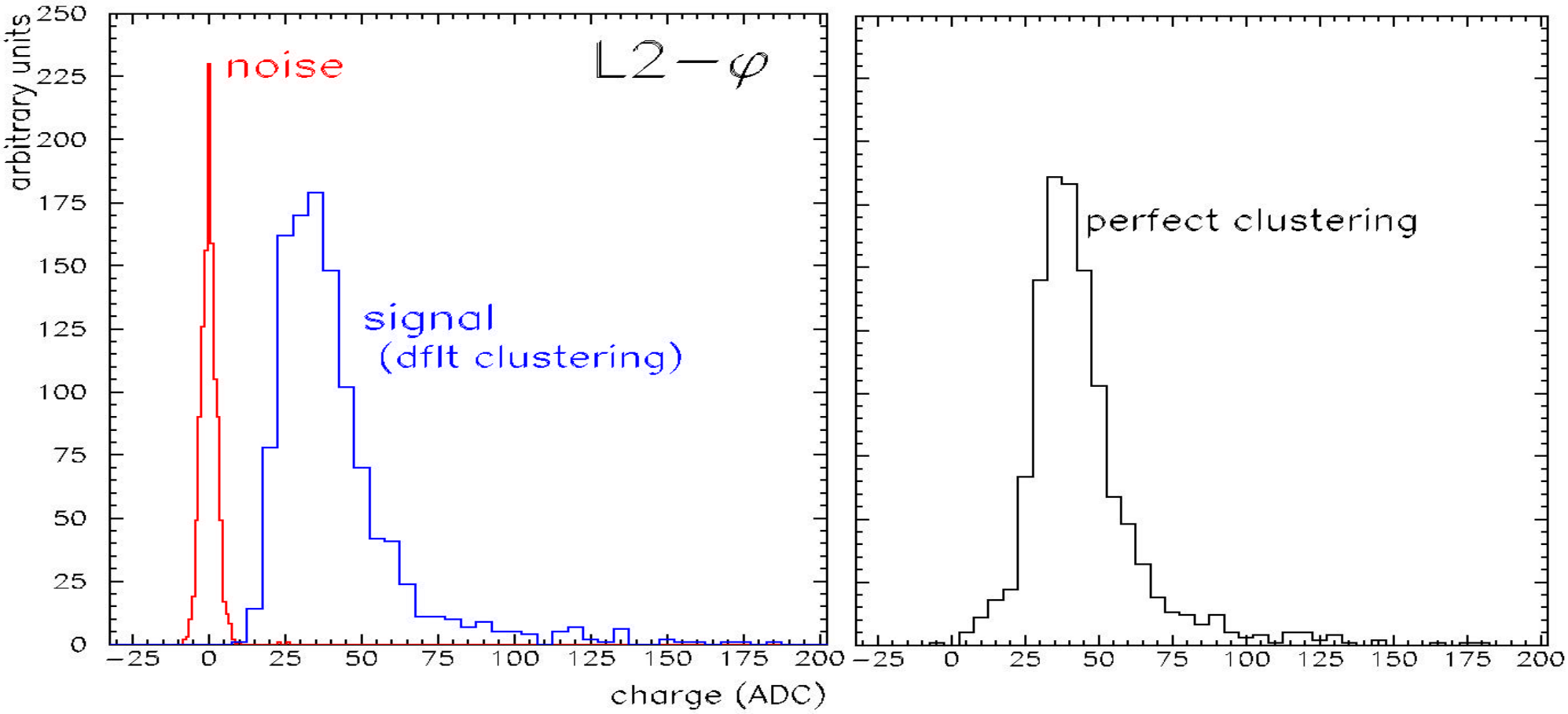
CLEO sensors have p-strips directly coupled to readout. Can give S/N ~ 50 if it works.

Clustering Studies



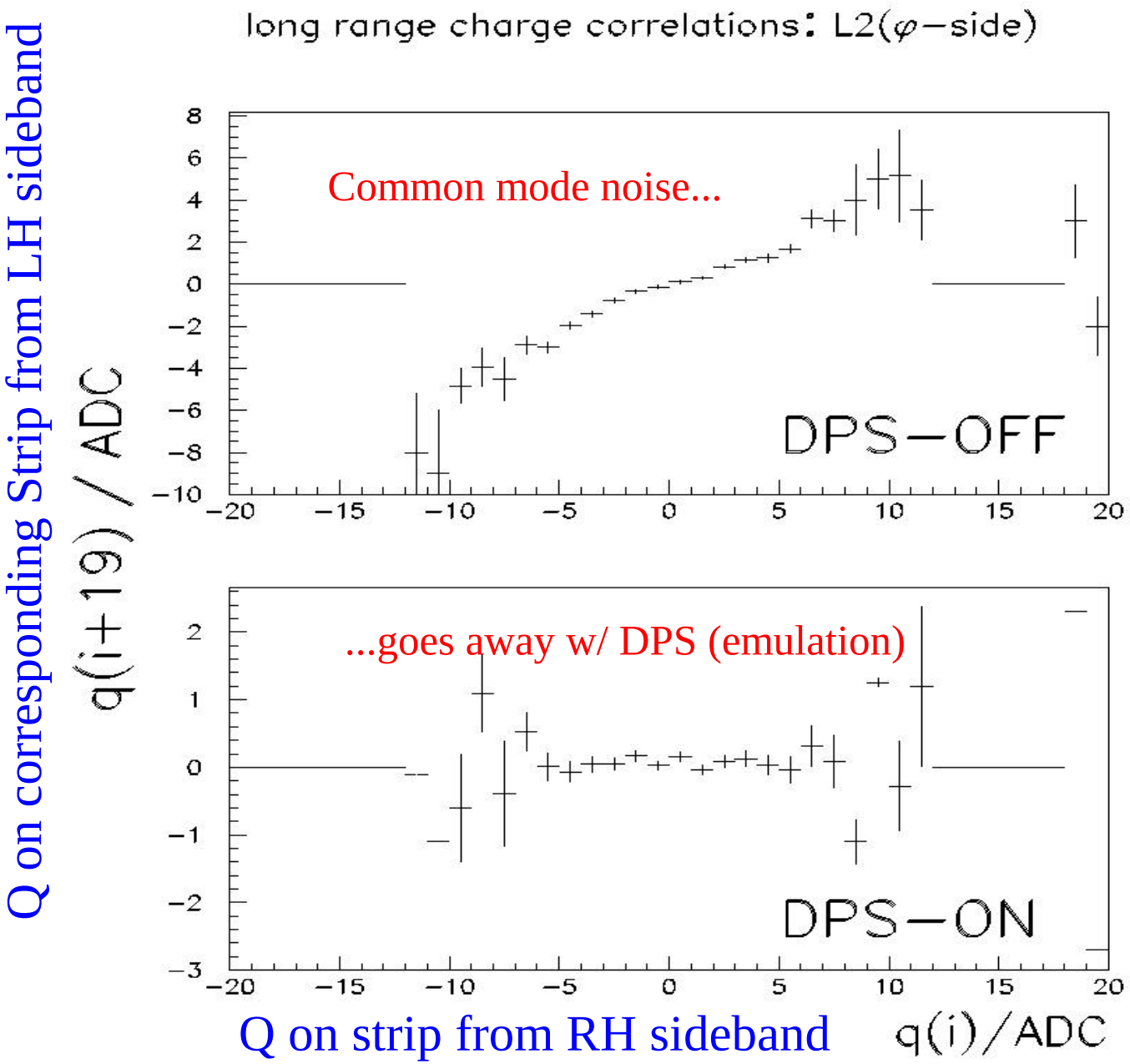
- Put a ladder (SB3W8) in Readall mode.
  - No Dynamic Pedestal Subt,
  - No threshold applied
  - All channels readout all the time.
- Produce unbiased clusters by removing layer under consideration from track pattern recognition.
- Make quality cuts on track, fiducial region, isolation in svx.
- Make signal and two sideband regions in silicon of 10 strips each.
- One Hammamatsu and one Micron ladder studied so far.

Are we collecting all the charge?



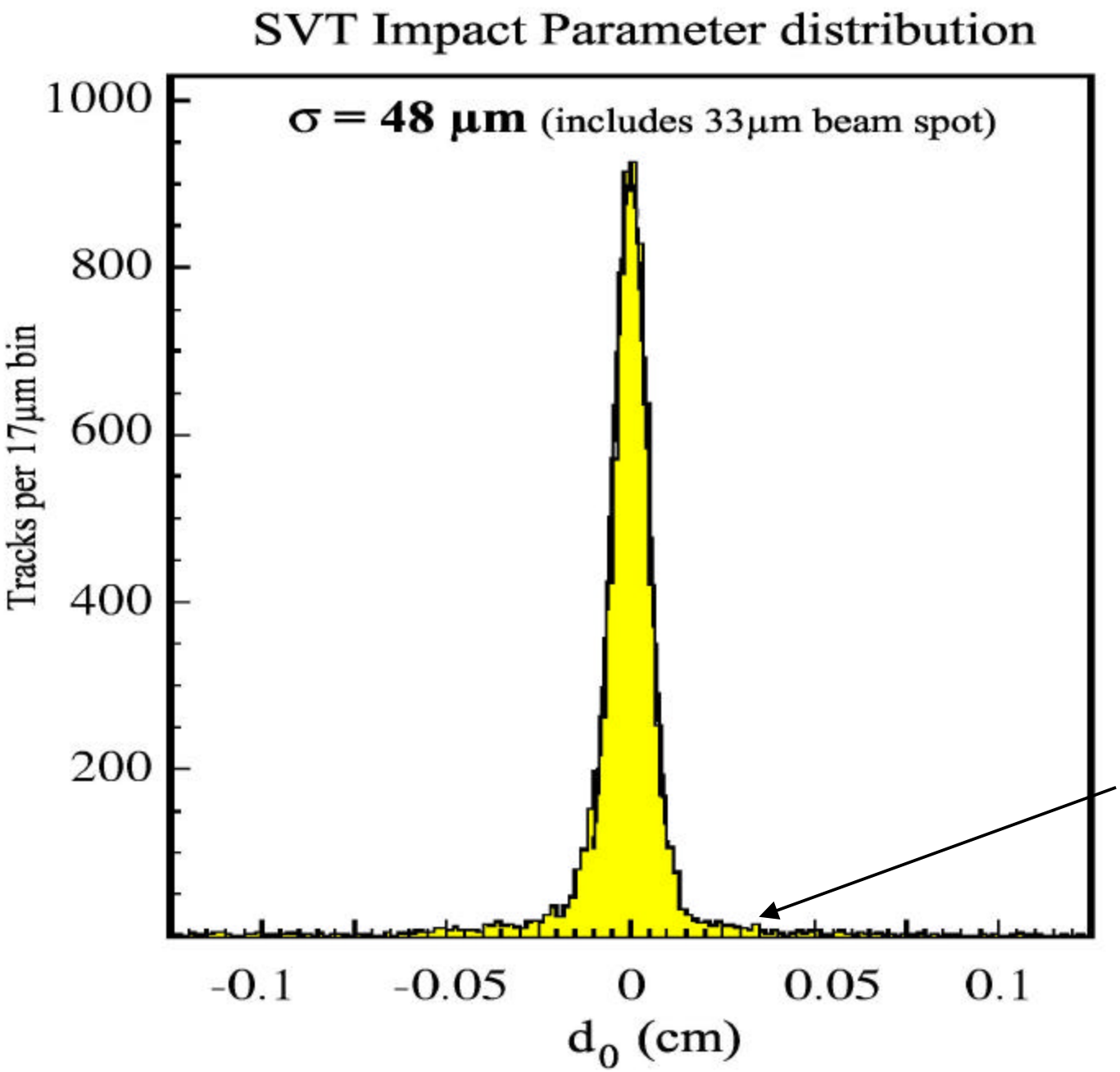
Noise from data runs (this study) is equal to noise from calib runs (default) to within 10%. Default clustering loses ~10% of the charge (difficult to recover). Both signal and noise are as expected.

Is Dynamic Pedestal Subtraction working?

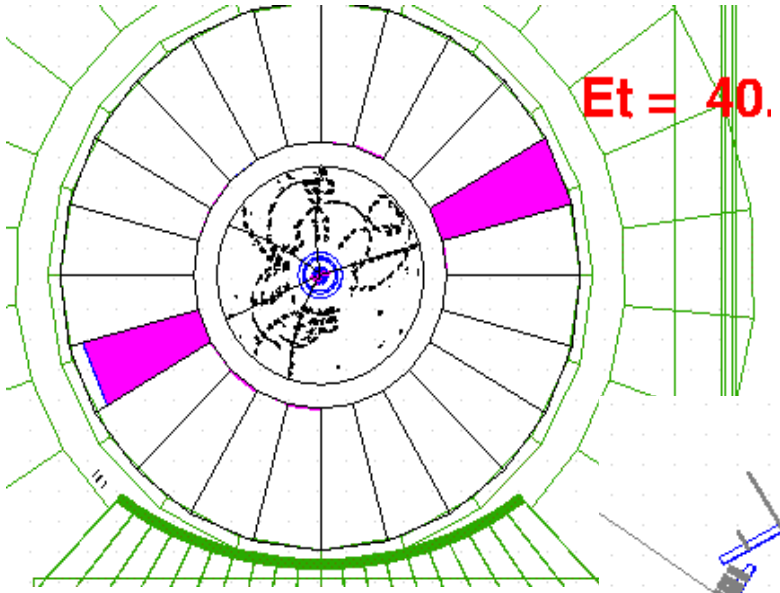


There is common mode noise on the strips, and DPS suppresses it efficiently.

Silicon Performance: Level 2 Trigger

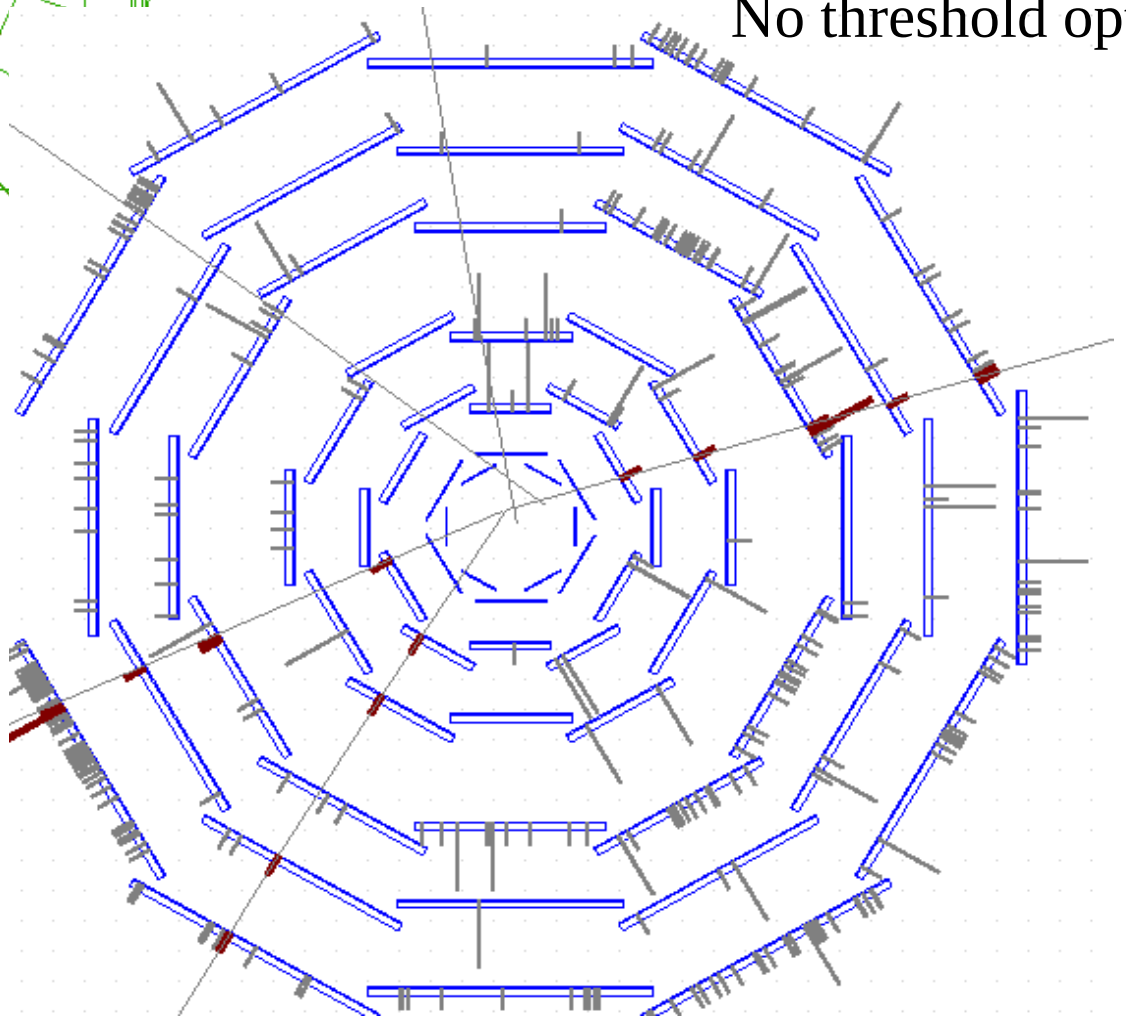


Tails should lessen with bad channel suppression.

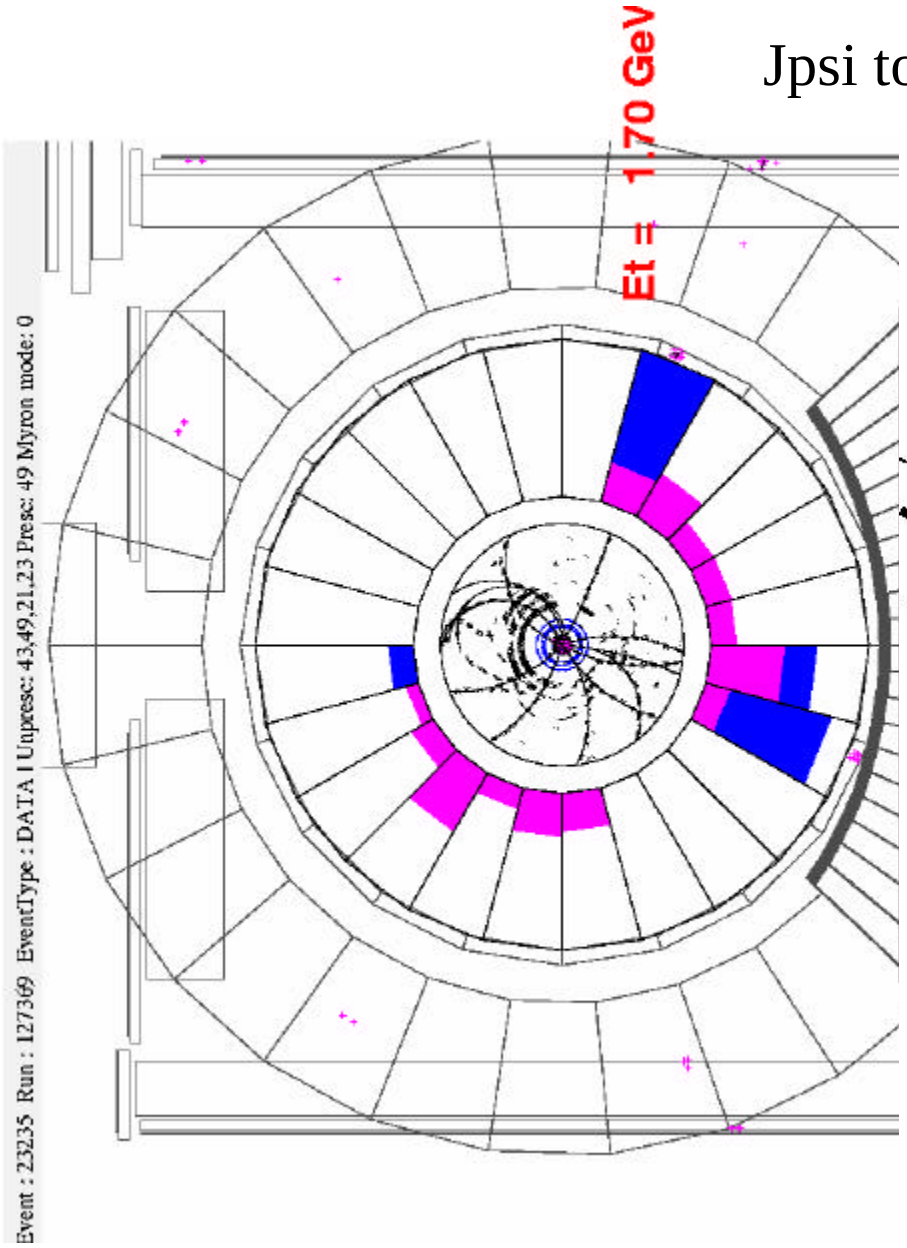


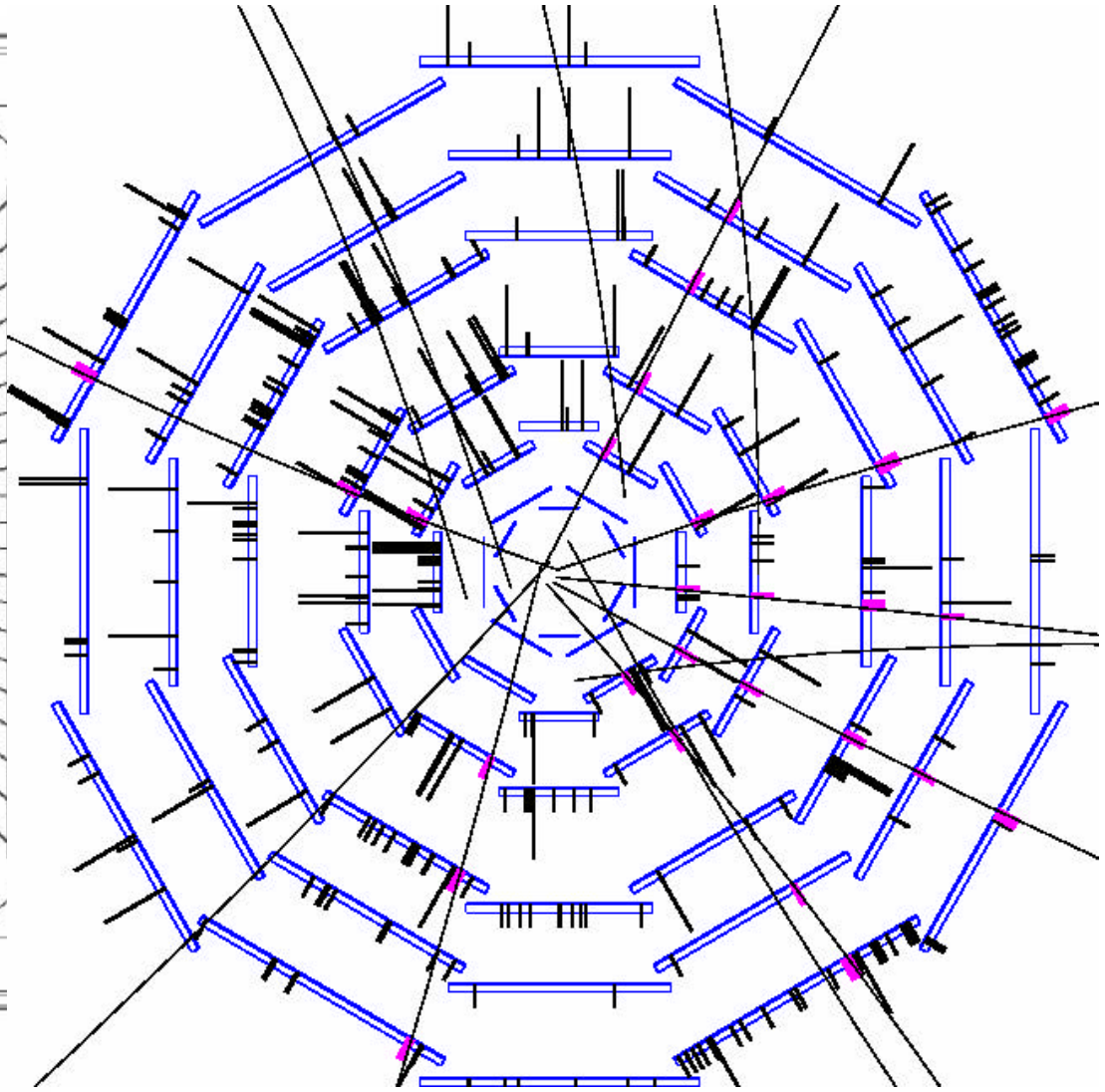
Z→ e+ e- event

SVX, all six ladders.
No threshold optimization.

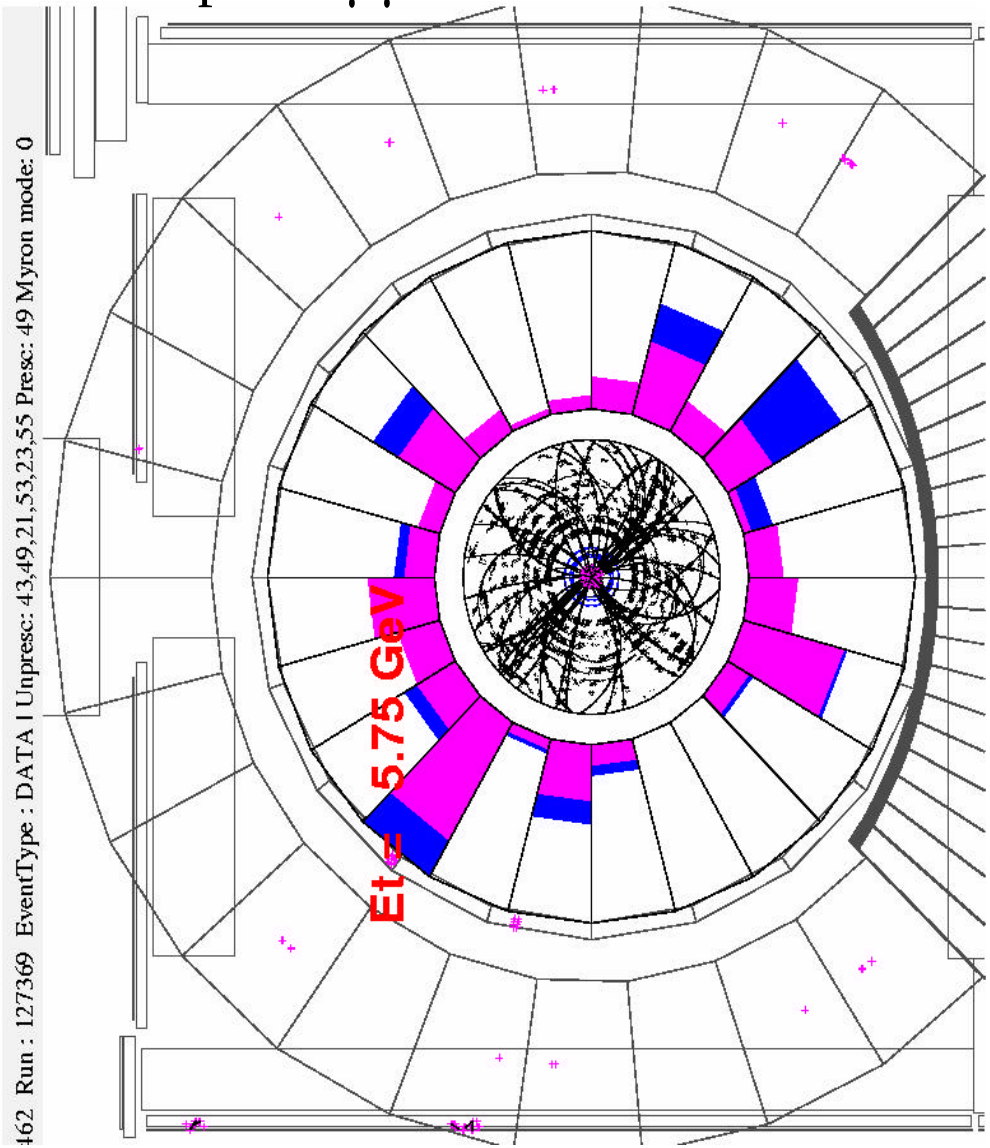


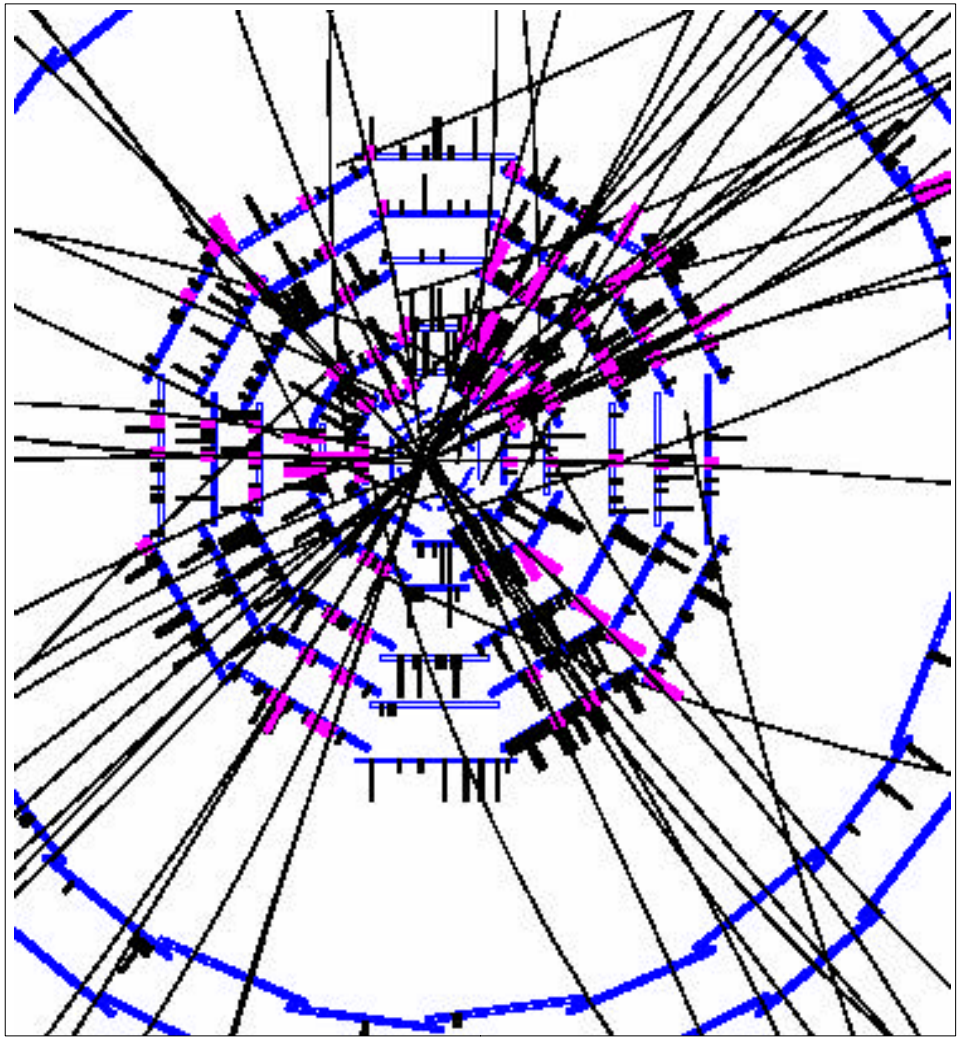
Jpsi to μμ event, M= 3.0507





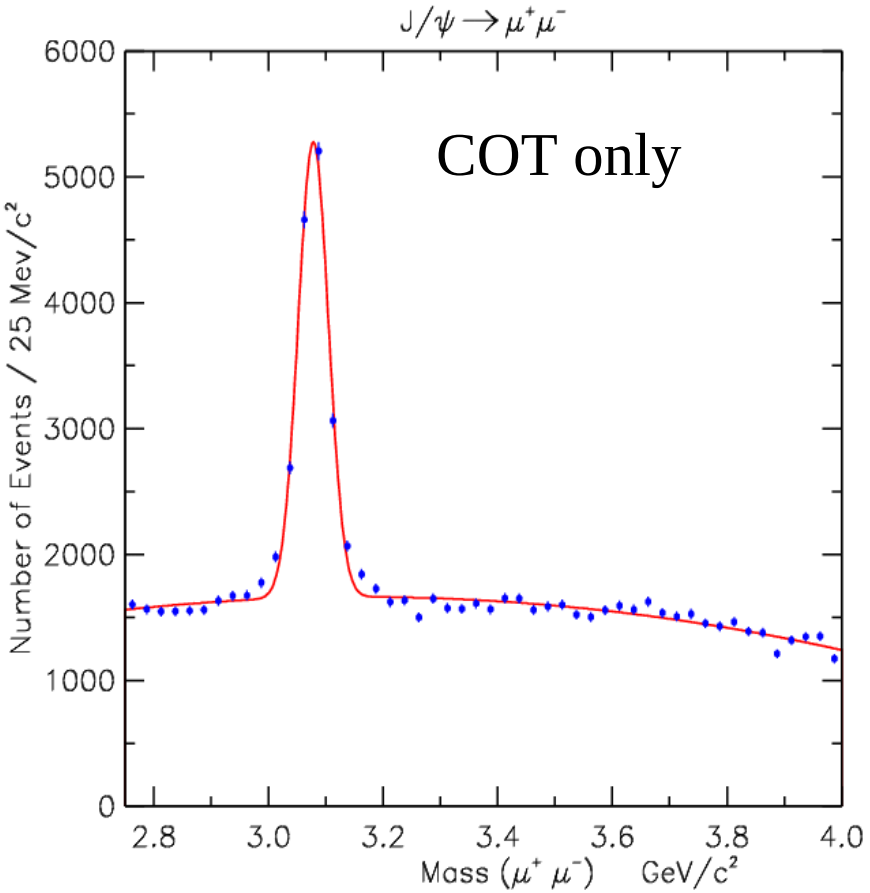
Jpsi to μμ event. M = 3.0859

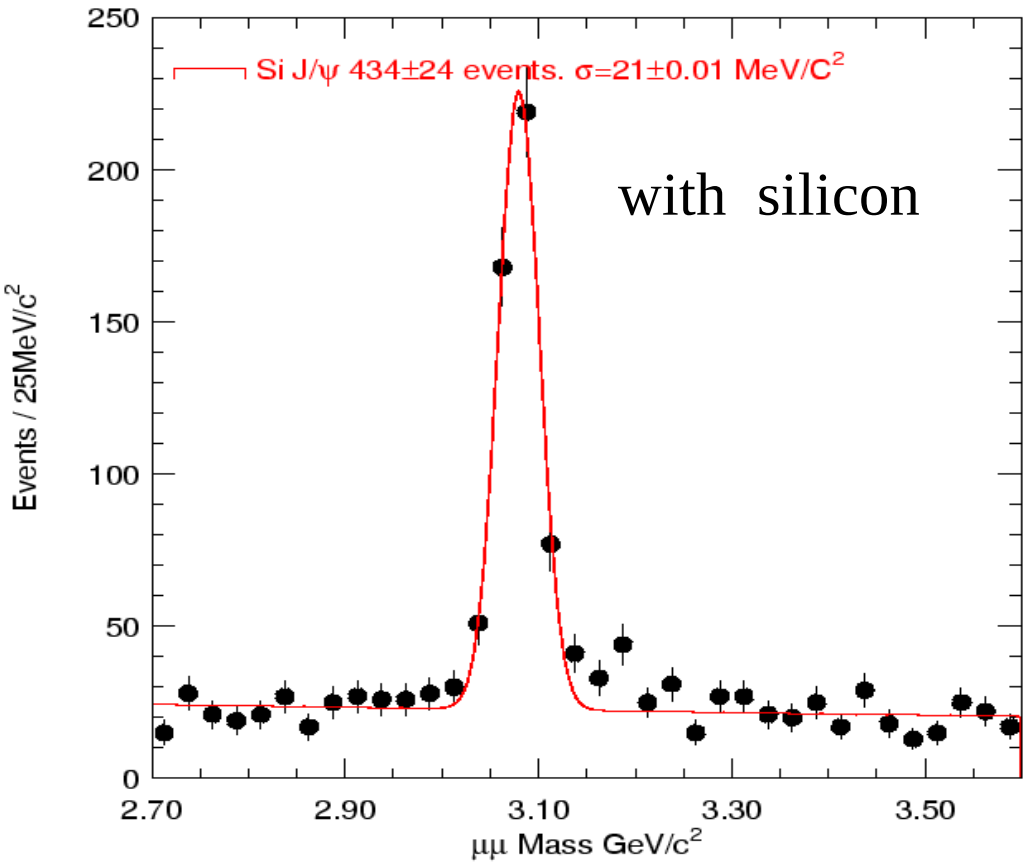




Andrei Loginov

Silicon used in preliminary physics analyses

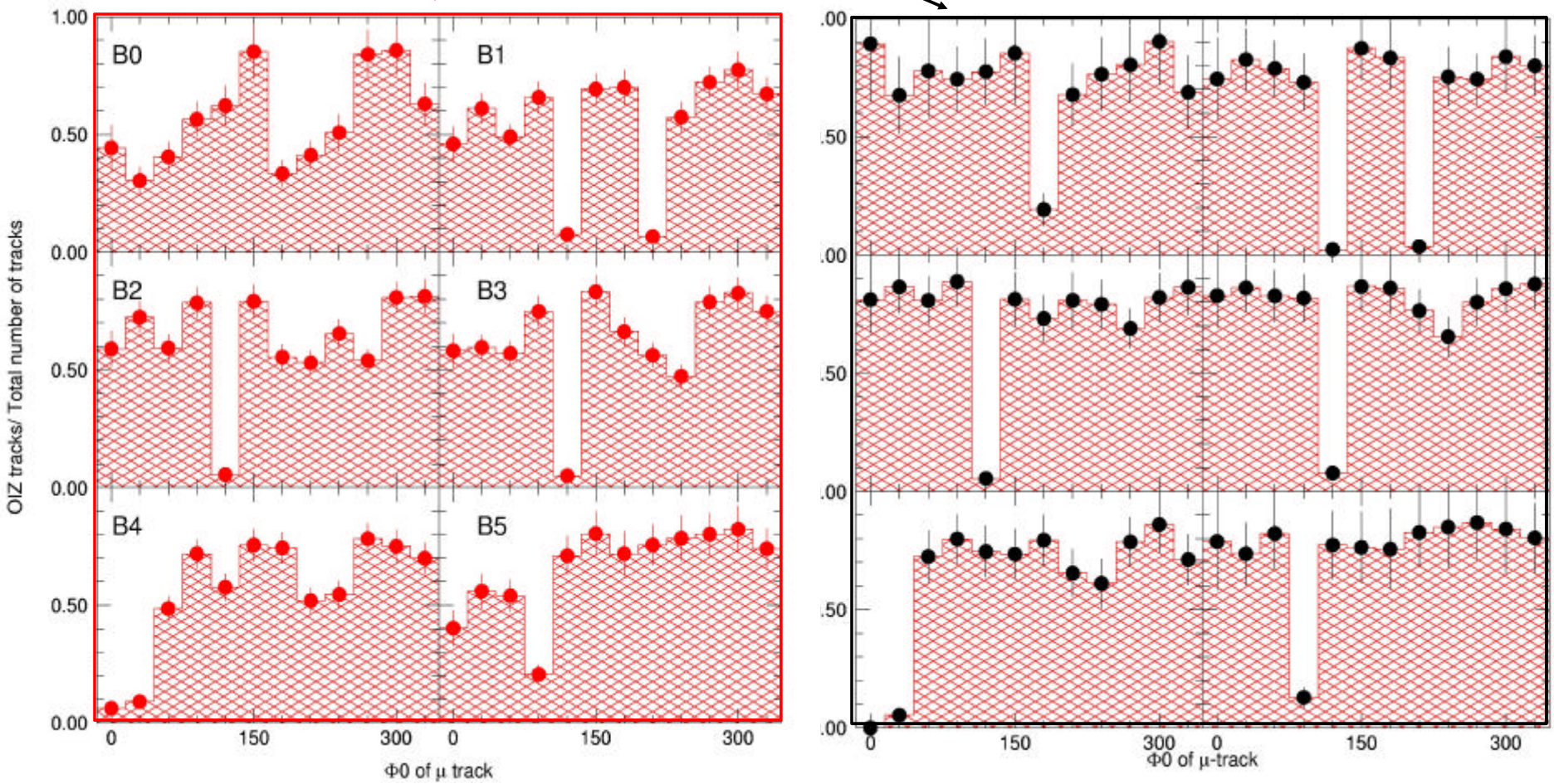




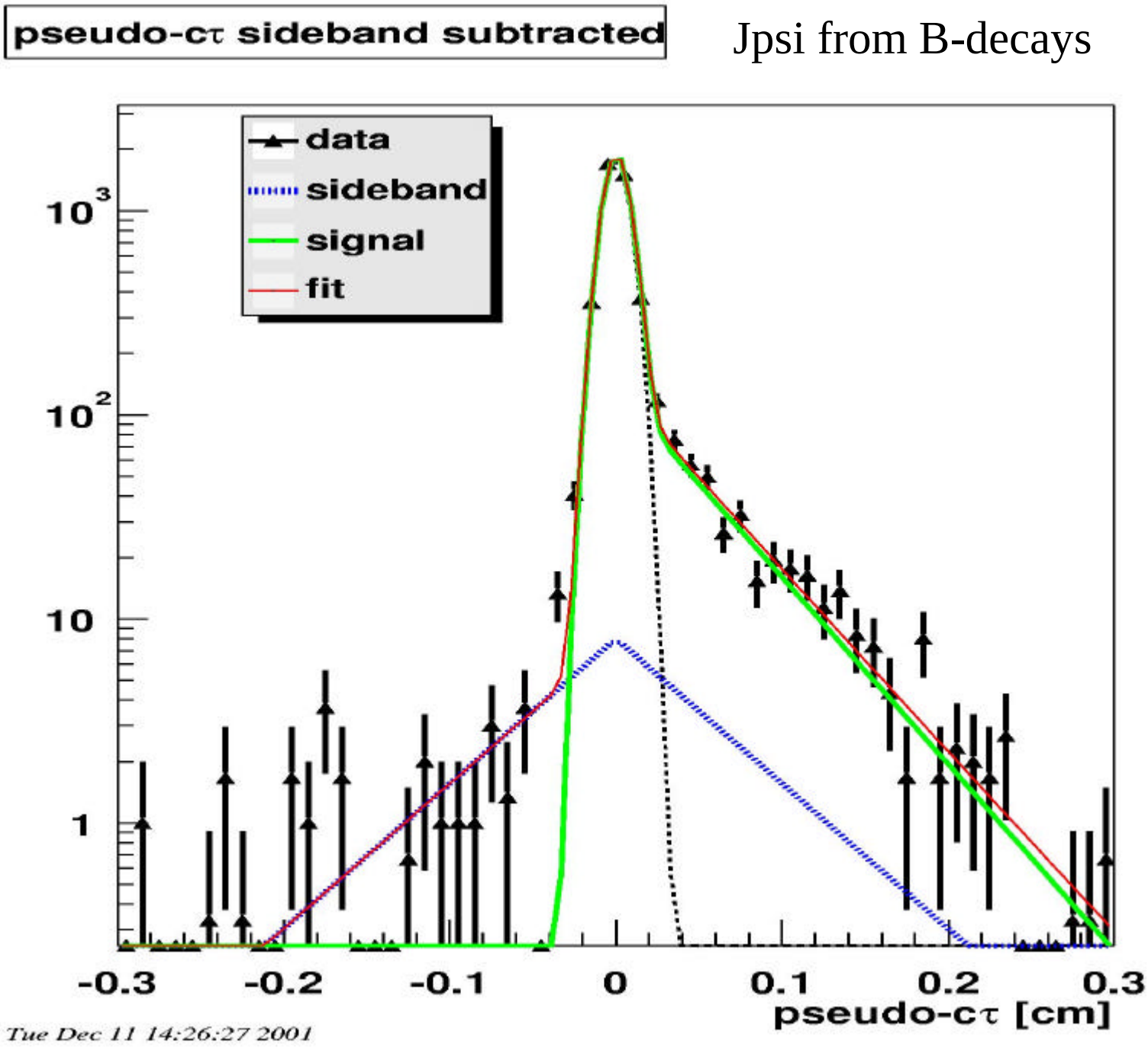
Silicon not aligned, several ladders not working in this dataset.

Alignment Matters.

Eff. Before and After prelim Alignment

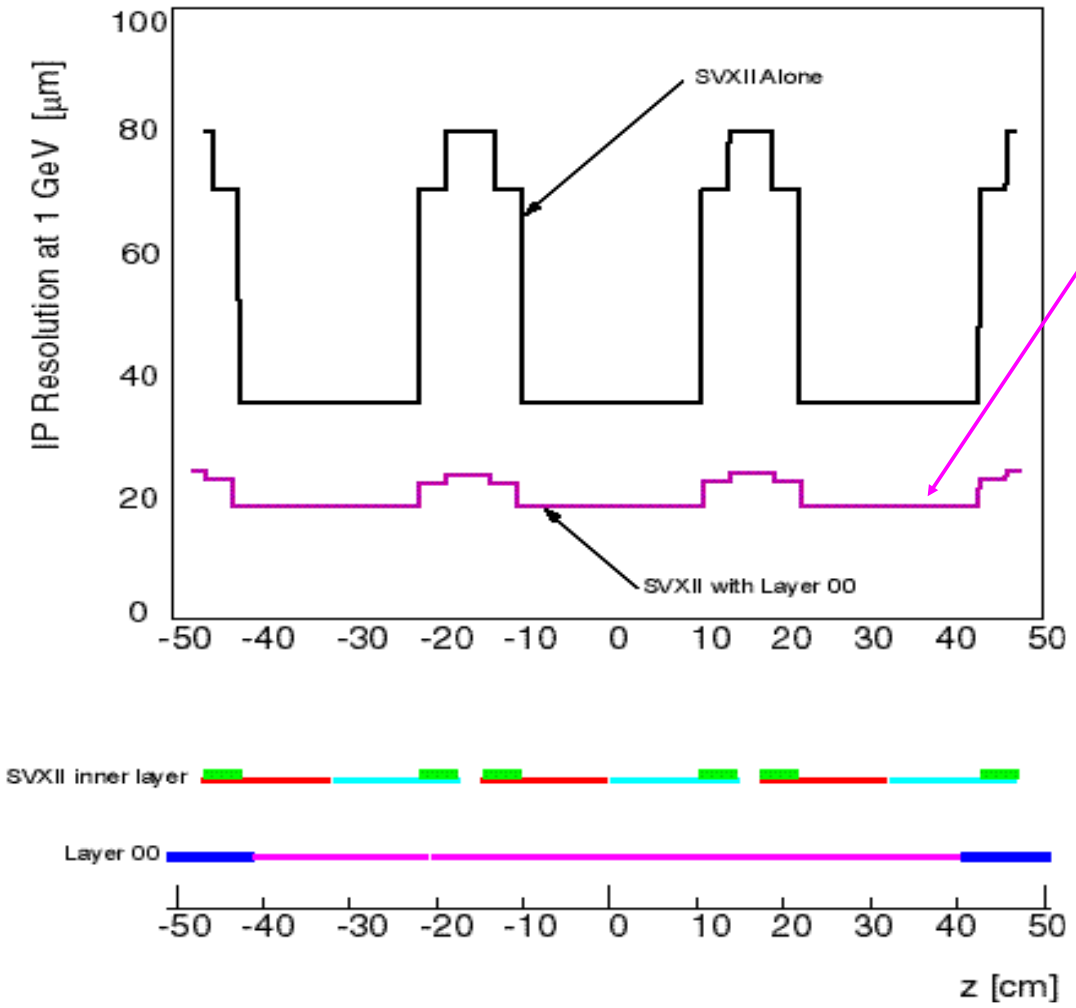


Basic Alignment only: barrel, wedge, ladder.
No sensor level (bows, twists, yaw, pitch...)

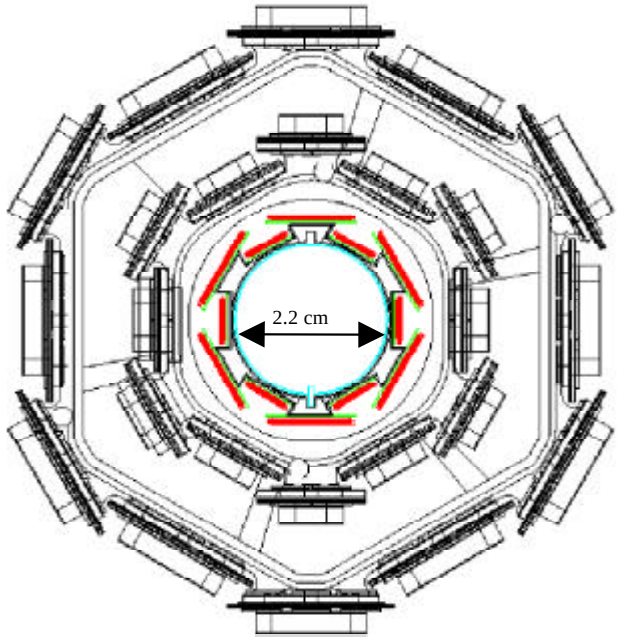


Jpsi from B-decays

Up Next: L00

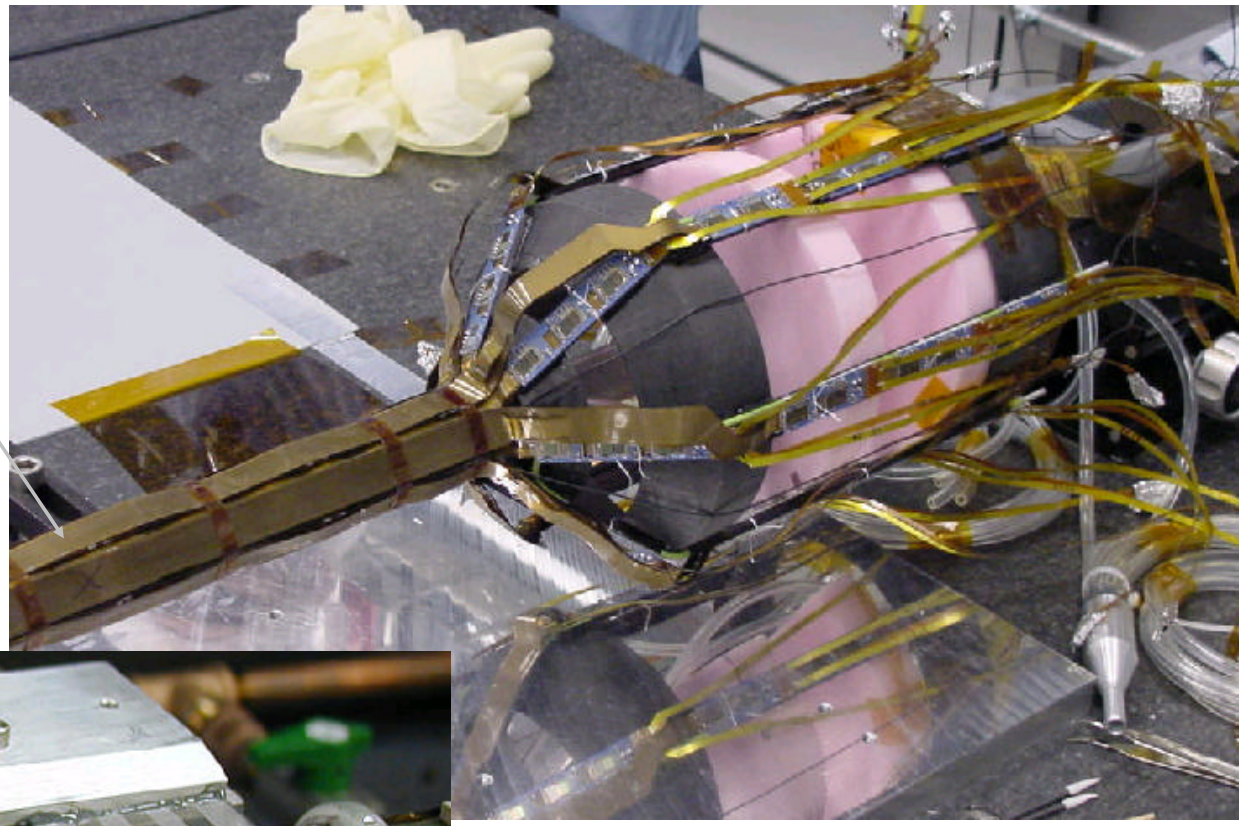


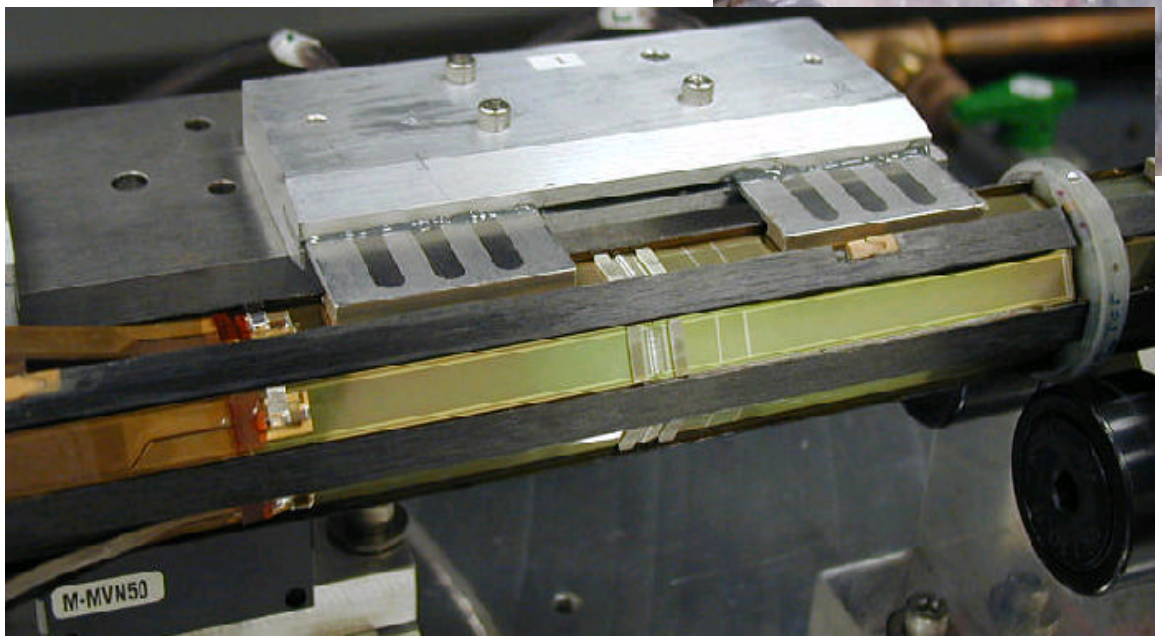
L00 promises to improve IP resolution by x2



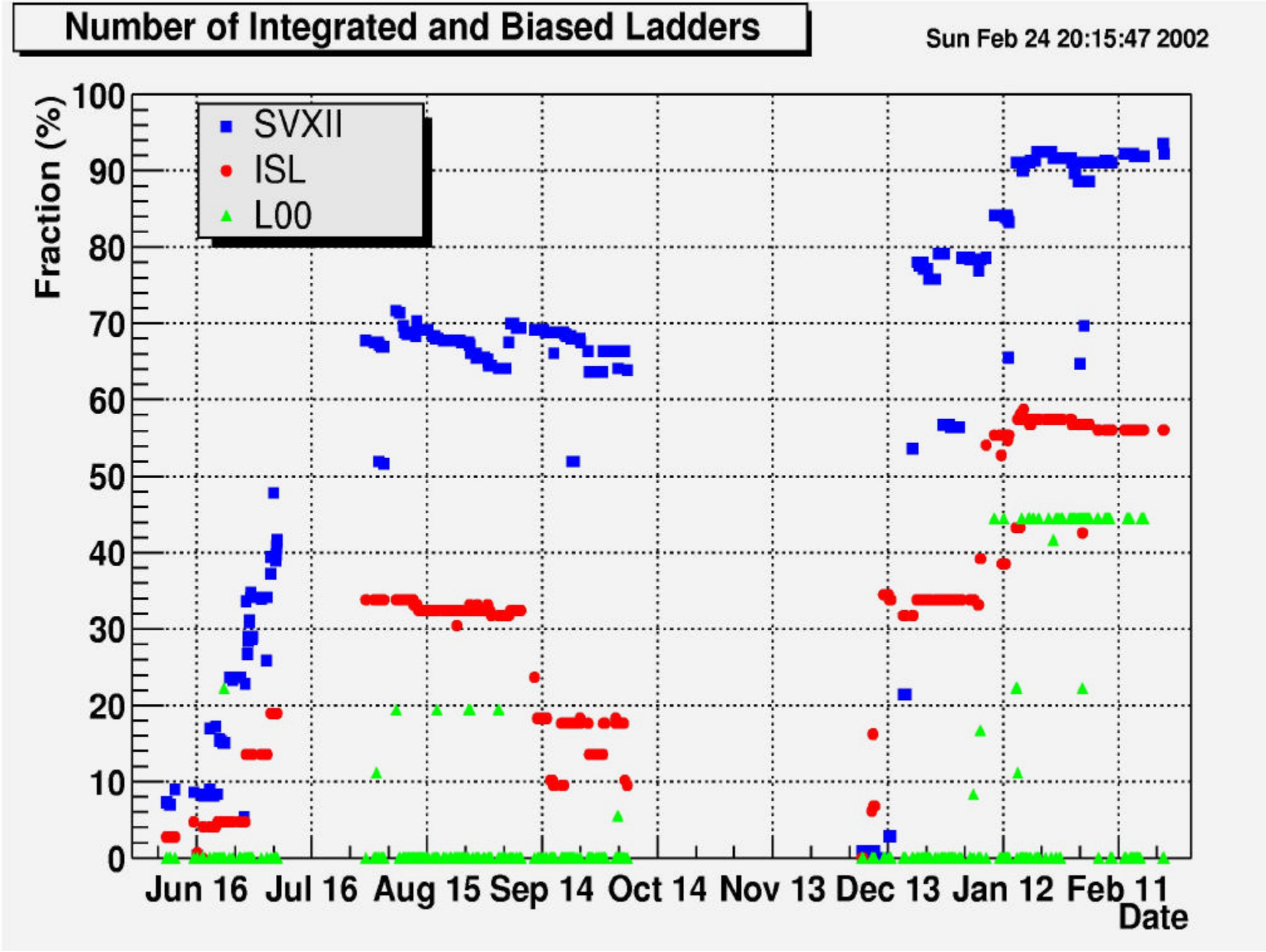
Layer00 Construction Issues

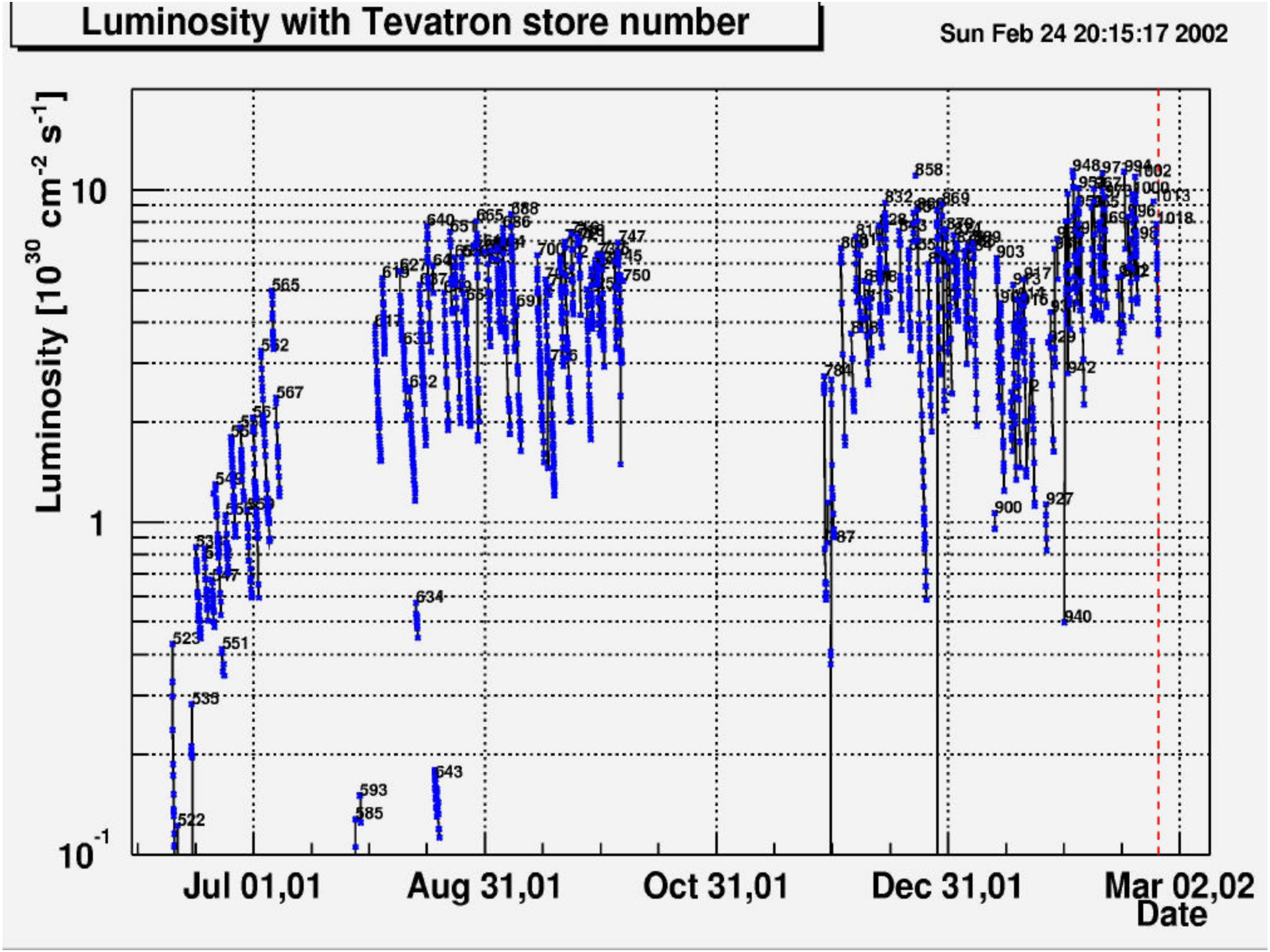
Cables, shielding, noise.





Some L00 ladders have large pickup noise that must be filtered out offline.


Number of Integrated and Biased Ladders
Sun Feb 24 20:15:47 2002
SVXII
ISL
L00
Fraction (%)
100
90
80
70
60
50
40
30
20
10
0
Jun 16
Jul 16
Aug 15
Sep 14
Oct 14
Nov 13
Dec 13
Jan 12
Feb 11
Date


Luminosity with Tevatron store number
Sun Feb 24 20:15:17 2002
Luminosity [10^30 cm^-2 s^-1]
10
1
10^-1
Jul 01,01
Aug 31,01
Oct 31,01
Dec 31,01
Mar 02,02
Date

CDF Silicon In Good Shape

- In 2000, CDF management was considering "de-scoping" measures.
  - Don't build Layer 4 (one of two SVX stereo layers).
- We elected to build the full detector, gambling that the Tevatron would turn on slowly, with lots of low luminosity running allowing us to commission. We won that gamble.
  - But commissioning a detector in "full publicity" mode is tough.
- Few large problems remain (ISL cooling, L00) but Silicon is mostly **ready for physics**.

Conclusion

- CDF Silicon is working. Some problems remain, work-arounds will be needed.
- Double-sided silicon is a hassle. *Let's not do it again*. Two separate sensors don't add much to the material budget.
- New detectors (CMS, Atlas) will have huge amounts of silicon. Boutique methods used so far will fail.
- SM, MSUSY Higgs within reach.
  Higgs working group neglected:
  - Layer 00.
  - Z tracking.
  - SVT in Level 2 Trigger.
- Let's find the Higgs before LHC turnon (CDF+D0 effort needed).