Electric Field Effect and FETs

- Electric Field Effect
- MOSFETs: band structure, depletion and inversion
- Long-channel MOSFETs

The Electric Field Effect

\[ E = \frac{V}{d_{\text{ox}}} \]

\[ en_{2D} = \varepsilon\varepsilon_0 E \quad n_{2D} = \frac{1}{e} \frac{4\pi\varepsilon\varepsilon_0}{4\pi} E \sim (10^8 - 10^9)E \]

Maximum \( E \) is limited by the dielectric breakdown (~\( 10^9 V/m \) for \( \text{SiO}_2 \), up to \( 10^{10} V/m \) for ionic gel gating)

(for comparison, \( \frac{e}{4\pi\varepsilon_0 a_B^2} \sim 10^{11} V/m \)).

\[ n_{2D}^{\text{max}} \sim 10^{19} \text{ m}^{-2} \text{ (conventional dielectrics)} \]

\[ 10^{20} \text{ m}^{-2} \text{ (ion gel).} \]

Electron concentration in a 1-nm-thick copper:

\[ 10^{29} \text{ m}^{-3} \times 10^{-9} \text{ m} = 10^{20} \text{ m}^{-2} \]

- the field effect is insignificant.

The situation is quite different in semi-metals and semiconductors.

Limitation of the ionic gel technique:
- cannot vary \( n_{2D} \) in-situ below the gel freezing \( T \sim 200 K \);
- polarization of the ionic gel is a slow (~1s) process.

The Field Effect (cont’d)

General Idea:

- to fabricate an artificial 2D system at the interface between the gate dielectric and a semiconductor/insulator with the charge density controlled by the gate;
- to study the charge transport in the system.

New states of matter can be explored with the field effect.


If the drain-source voltage $V_{DS}$ is small in comparison with the gate-source voltage $V_{GS}$, the charge carrier concentration is uniform along the channel.

Provided all $V_{GS}$ is applied btw the gate and the channel:

\[
\frac{n_{2D}}{e} = \frac{C_{di} (V_{GS} - V_T)}{-e}
\]

$C_{di}$ is the gate dielectric capacitance per unit area.

More accurately, taking into account the voltage divider $C_{di}, C_{sc}$:

\[
n_{2D} = \frac{\frac{C_{di} C_{sc}}{C_{di} + C_{sc}} (V_{GS} - V_T)}{-e}
\]

$C_{SC}$ - the semiconductor space-charge capacitance

$V_T$ - the threshold voltage. It is proportional to the density of charge traps at the $Si-SiO_2$ interface. There are no mobile charges in the channel unless $V_{GS}$ is greater than $V_T$. The early history of MOSFET development was the struggle to reduce $V_T$.

Why $Si$? Because the processes of elimination of charge traps in the bulk of thermally grown $SiO_2$ and at the the $Si - SiO_2$ interface have been developed.
Early History of Si MOSFETs

Julius Lilienfeld proposed FET, but never constructed a working device...

Martin M. (John) Atalla (1924 – 2009)
Dawon Kahng (1931 – 1992)

Julius E. Lilienfeld (1882 –1963)

Shockley and Brattain attempted to make FET, but failed...

Fred Heiman and Steven Hofstein

Oskar Heil

attributed the failure of Shockley’s efforts to the surface states


D. Kahng, M. Atalla (Bell)
S. Hofstein, F. Heiman (RCA Sarnoff) created practical Si FETs

Michael Riordan & Lillian Hoddeson. “Crystal Fire: The Invention of the Transistor and the Birth of the Information Age”.

Martin M. (John) Atalla (1924 – 2009)
Dawon Kahng (1931 – 1992)
Electric Field Effect

MOSFETs: band structure, depletion and inversion

- Long-channel MOSFETs

- Two types of FETs developed at Rutgers:
  - single-crystal organic FETs (OFETs)
  - transition metal dichalcogenide FETs
We’ll consider just one type of FETs (an $n$-type $Si$-based MOSFET). Many more types of FETs exist, both $n$- and $p$-type, with inversion and accumulation channels, “normally-on” and “normally-off”, inorganic and organic, etc.
Let’s first consider the case when the gate and the semiconductor are electrically isolated.

The holes are primary carriers in the $p$-doped Si

Chemical potentials are not aligned yet.
The gate and the semiconductor are electrically isolated.

The gate and the semiconductor are electrically connected $V_{GS} = 0$.

To line up chemical potentials, charges are redistributed through an external circuit. As the result (a) the bands bend near the $Si - SiO_2$ interface, (b) the region near the interface is depleted of holes, primary carriers in the $p$-doped $Si$.

The total built-in voltage $V_{bi} = \frac{1}{e} |\Phi_G - \Phi_S|$ where $\Phi_G$ and $\Phi_S$ are the work functions of the gate and semiconductor, respectively. This voltage drops across the oxide and the depletion region.
nMOSFET band diagram (from Gate to Channel) $V_{GS} \neq 0$

Minority Carriers (electrons) form an inversion layer at the $Si - SiO_2$ interface.
Figure 1.5  Normalized total semiconductor charge per unit area versus normalized surface potential for p-type Si with \( N_e = 10^{16} \text{cm}^{-3} \), \( Q_{th} = (2e_q N_e V_{th})^{1/2} \approx 9.3 \times 10^{-9} \text{C/cm}^2 \) and \( V_{th} \approx 0.026 \text{V} \) at \( T = 300 \text{K} \). The arrows indicate flat-band condition and onset of strong inversion.

\[
\begin{align*}
C_{di} & - \text{the gate dielectric capacitance} \\
C_{SC} & - \text{the semiconductor space-charge capacitance} \\
C_{IT} & - \text{the interface trap capacitance}
\end{align*}
\]
MOSFET: degenerate or non-degenerate?

Operation at 300K – we need to compare \( k_B T \) with \( E_F(n_{2D}) \).

\[
n_{2D} = \frac{\varepsilon \varepsilon_0}{e t_{ox}} V = (\varepsilon = 4, t_{ox} = 2nm, V = 0.8V) = 8 \times 10^{16} m^{-2}
\]

\[
E_F(n_{2D}) = \frac{\hbar^2}{m^*} \pi n_{2D} \quad m^* = 0.2m_e
\]

\( n_{2D} = 10^{16} m^{-2}, \quad E_F(n_{2D}) \approx 100K \) - non-degenerate Fermi gas

\( n_{2D} = 10^{17} m^{-2}, \quad E_F(n_{2D}) \approx 1000K \) - (almost) degenerate Fermi gas
Electric Field Effect

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Two types of FETs developed at Rutgers:
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Field-Effect Transistor (FET) geometry
MOSFET Current-Voltage Characteristics and Modes of Operation

**Analog applications**
MOSFETS as amplifiers

**Digital applications**
MOSFETS as switches

\[ V_{DS} = V_{GS} - V_T \]

I_{SD} (arb. units) vs. V_{SD} (V)

- **Subthreshold regime**
  \[ V_{GS} < V_T \]

- **“Linear” regime**
- **Saturation regime**
The Linear Regime

- describes the MOSFET behavior for small $V_{DS}$, where the MOSFET acts as a variable resistor. $\mu, n_{2D}, E_{DS}$ are considered constant along the channel.

$$E_{DS} = \frac{V_{DS}}{L} \quad n_{2D} = \frac{C_{di}(V_{GS} - V_T)}{-e} \quad |V_{DS}| \ll (V_{GS} - V_T)$$

$C_{di}$ is the gate dielectric capacitance per unit area.

$$j_{DS} = (-en_{2D}\mu)E_{DS} = -e \frac{C_{di}(V_{GS} - V_T)}{-e} \mu \frac{V_{DS}}{\sigma_{2D}}$$

$$I_{DS} = Wj_{DS} = \mu C_{di}(V_{GS} - V_T) \frac{W}{L} V_{DS}$$

To increase $I_{DS}$, we need higher mobility and lower $V_T$. Greater $C_{di}$ (i.e. larger $n_{2D}$) also helps, though the $RC$ time constant increases (not good, lower operation frequencies).
The Drain Current Saturation Regime

For larger $V_{DS}$ comparable with $V_{GS} - V_T$ we have to take into account variations of $n_{2D}$ along the channel. The guiding principle – the continuity equation, $j_{DS}$ is the same in any cross section.

$$j_{DS}(x) = (-en_{2D} \mu)E(x) = \mu C_{di} (V_{GS} - V_T - V(x)) \frac{dV(x)}{dx}$$

$$j_{DS}(x) = j_{DS} = \text{const}$$

$$\int_0^L j_{DS} dx = \mu C_{di} \int_0^{V_{DS}} (V_{GS} - V_T - V(x)) \frac{dV(x)}{dx} dx$$

$$j_{DS}L = \mu C_{di} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{DS} = \mu C_{di} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$I_{SD}$ increases linearly for small $V_{DS}$, but then reaches a maximum when $n_{2D}$ becomes zero at the drain end of the channel. Holes are separated from the channel by the depletion layer and cannot contribute to $I_{SD}$. $I_{SD}$ saturates and the depletion layer near the drain end of the channel accommodates the “excessive” $V_{DS}$.

$$I_{DS,sat} = \mu C_{di} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} \quad V_{DS} > V_{GS} - V_T$$
The Quadratic Model, Drain Current Saturation (cont’d)

The characteristics of an ideal FET.

**OFF state** - $V_{GS} < V_T$.

**ON state** - $V_{DS} > V_{DS}^{sat}$, saturation regime.

Saturation regime is of primary importance for digital applications, where the output current of a FET should only depend on the input (gate) voltage and not on $V_{DS}$.

In the pinch-off regime, $E$ at the source is independent of $V_{DS}$. $I_{DS}$ also becomes independent of $V_{DS}$ (continuity equation).
Desirable FET Characteristics

- Small $V_T$ and $V_{ON} - V_{OFF}$ (steep subthreshold slope) $\Rightarrow$ small energy dissipation

- **ON/OFF current ratio** $> 10^4$ $\Rightarrow$ heating minimization in the OFF regime, small energy dissipation

- Well-defined saturation regime
- Electric Field Effect
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Single-Crystal Organic FETs

- **Si, Ge, GaAs**
  - Strong covalent bonding
  - Large ($\sim 10$ eV) bandwidth
  - High mobility of electrons and holes, $\mu \sim 1000$ cm$^2$/Vs

- **Conjugated polymers and small-molecule organic semiconductors**
  - Weak van der Waals bonding
  - Narrow ($\sim 0.1$ eV) bandwidth
  - Low mobility of carriers, $\mu \sim 0.1 - 10$ cm$^2$/Vs

Wanted: flexibility + reasonably high $\mu$
Single-Crystal Organic FETs (cont’d)

Organic FETs work in the *accumulation* regime. Van-der-Waals bonding between the molecules – *low density of surface traps*.

Mobility – up to 20 cm$^2$/Vs, 10 times greater than in the best organic TFTs and α-Si:H MOSFETs, is *independent* of $V_{GS}$ (i.e. $n$) and $V_{DS}$ (i.e. $E$) - in contrast to the polymer and α-Si:H TFTs. Most importantly, this is the intrinsic (not trap-limited) $\mu$.

On/off ratio – up to $10^7$

Sub-threshold slope – 10 times better than in organic TFTs and α-Si:H MOSFETs.

These results have been recognized by Scientific American as one of the major contribution to the development of flexible electronics in 2005.


World’s fastest organic transistors, Rutgers 2003
Single-crystal Organic Semiconductor *Rubrene* \((C_{42}H_{28})\): the intrinsic (defect-free) mobility

H.H. Choi,... V. Podzorov. Critical assessment of charge mobility extraction in FETs. 
### FETs based on *Layered* Inorganic Semiconductors

<table>
<thead>
<tr>
<th>strong covalent/ionic bonds</th>
<th>weak van der Waals bonds</th>
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<tbody>
<tr>
<td>high mobility,</td>
<td>low mobility,</td>
</tr>
<tr>
<td>lots of surface states</td>
<td>few surface states</td>
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**Transition Metal Dichalcogenides** - $MX_2$, where $M$ stands for a transition metal and $X$ - for Se, S or Te. Layered semiconducting TMDs – an ideal FET material, “the best of both worlds”: covalent/ionic bonding within the layers $\equiv$ high mobility, + weak van der Waals interlayer bonding $\equiv$ no dangling bonds, low $V_T$

$$\mu_p \ (300K) \sim 500 \ cm^2/Vs$$
- comparable or even better than the RT mobility of electrons in commercial Si MOSFETs